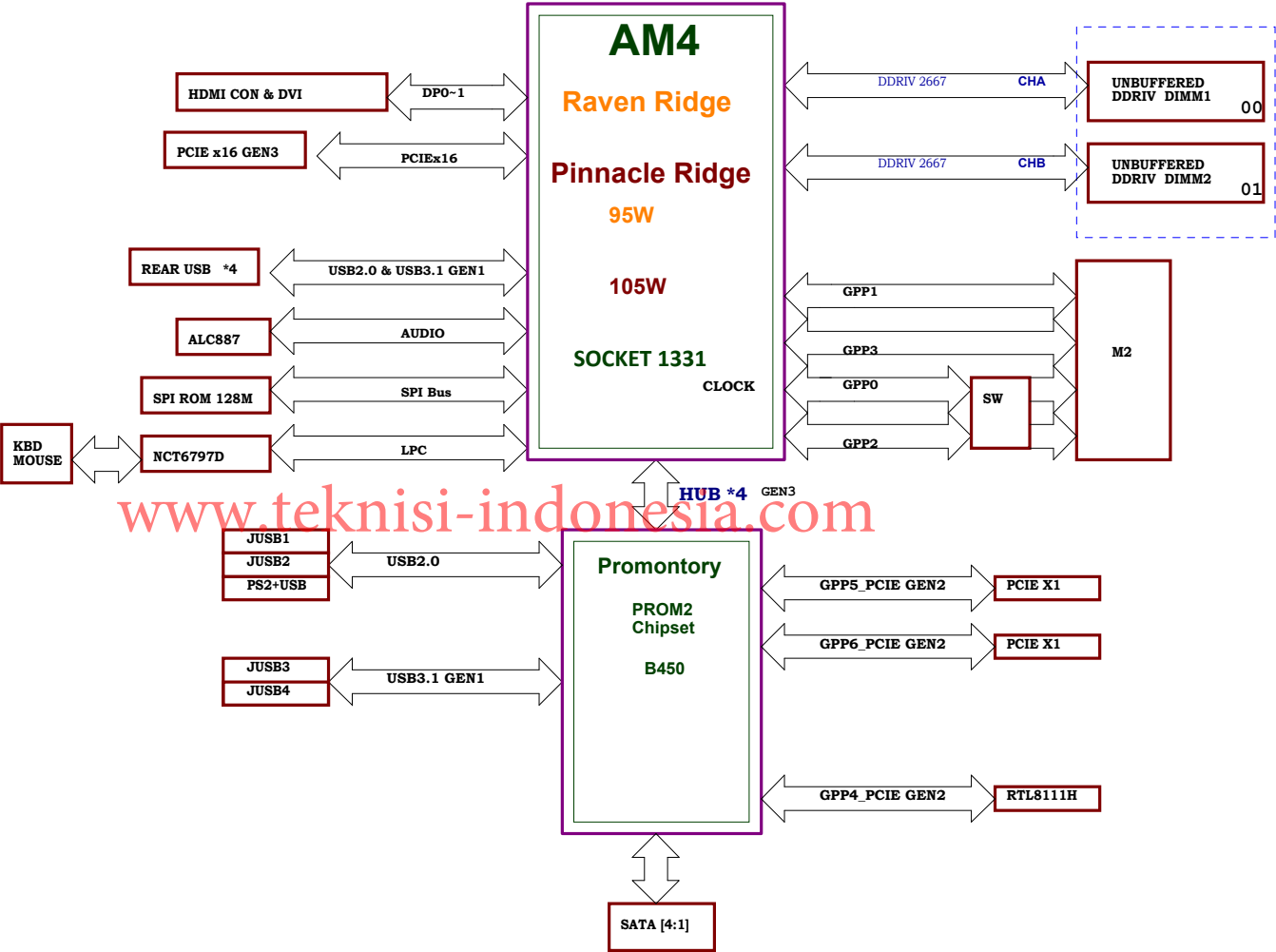


MS-7B87 Ver:11

- CPU:**
AMD AM4
- System Chipset:**
Promontory B450
(Value DIY or System Builder)
- Main Memory:**
DDR IV * 2 MAX:32 GB
- VRM**
RT8894 4+2
- On Board Chipset:**
LPC Super I/O --NCT6797D-M
LAN RTL8111H
Azalia CODEC - Realtek ALC887
- Expansion Slots:**
From CPU
PCI Express X16 Slot * 1
PCI Express X1 Slot * 1
PCI Express X1 Slot * 1
M2_2 * 1
- OCP IC:**
RT9553B

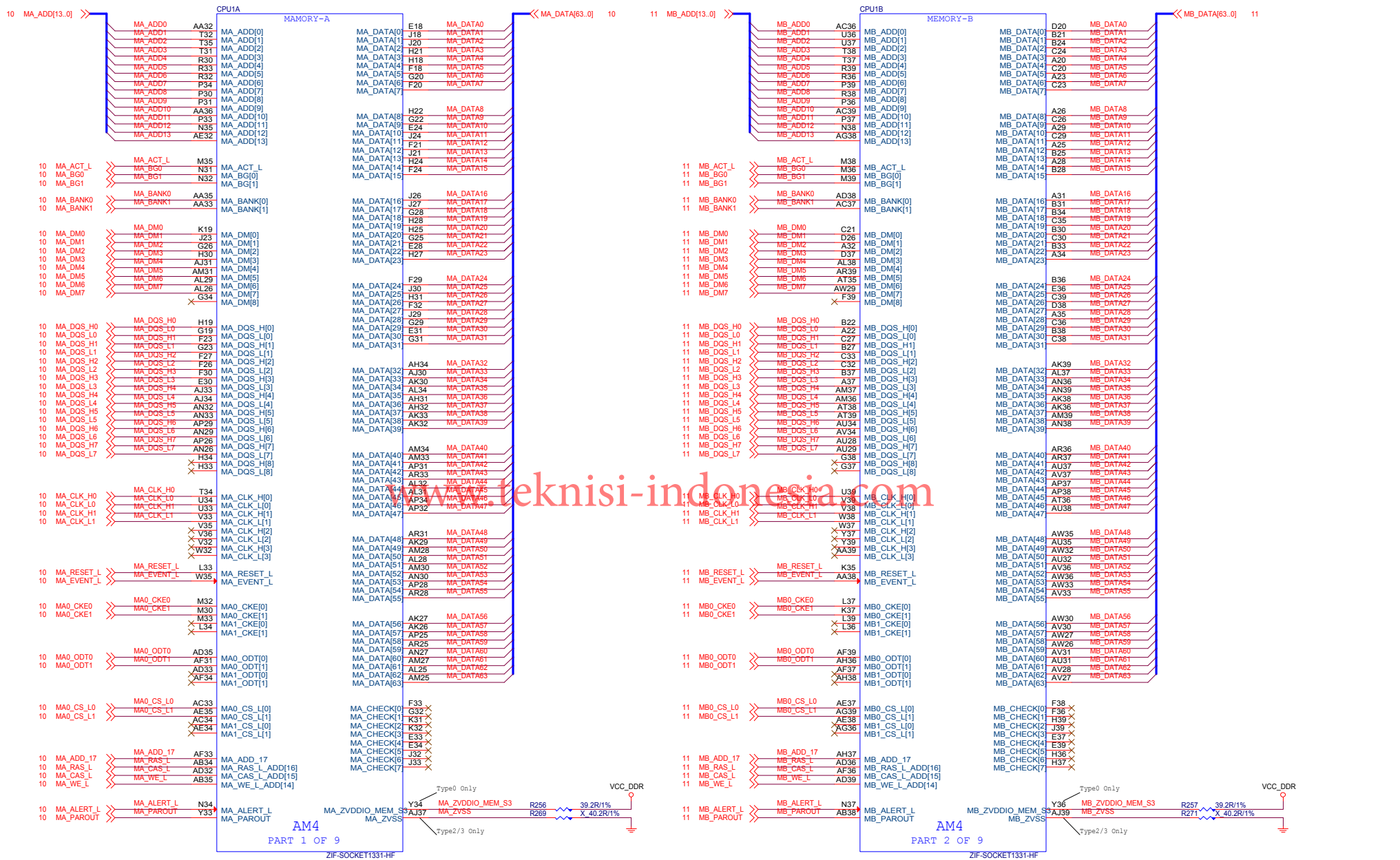
FUSION BLOCK DIAGRAM



AMD AM4

01 Block Diagram	38 CPU Power 1P8V-MP2147
02 Cover Sheet	39 CPU Power VDDP-MP8712
03 FM4 DDR4 I/F	40 CPU Power Connector/PWRGD
04 AM4 PCIE/SATAE	41 CPU Power RT8894 3+2 Phase
05 AM4 Display/Audio	42/43 CPU Power Phase 1-4
06 AM4 SVI/ACPI/GPIO	44 CPU Power NB Phase 1-2
07 AM4 LPC/SPI/USB/CLK/STRAP	45 CPU Power NB Switch/NCT3933
08 AM4 Power/RTC Power/ 09 AM4 GND	46 RT9553B CURRENT SENSE
10,11 DDR4-DIMM CH-A/B	47 ATX/Front Panel
12,13 DDR4-POWER/GND	48 ALL LED Control
14 Promontory-PCIE/SATA/SATAE	49 JRGB1/JRGB2
15 Promontory-USB/OC	50 BOM Option
16 Promontory-CLK/ACPI/GPIO	51 RTC Circuit/Moat Cap
17 Promontory-Power / 18 Promontory-GND	52 M2_2
19 PCIE X16(X1*2) SLOT	53 History
20 SIO NCT6797D	54 Power Sequence
21 SIO HWM/COM	55 Power Delivery
22 DVI Connector	56 GPIO MAP
23 FAN Control TYPE L/ K	
24 / 25 / 26 LAN-RTL8111H/Audio ALC887	
27 USB Rear PS2+USB2.0	
28 USB Rear LAN+USB3.1 GEN1	
29 Rear USB3.1 Type C / mux	
30 USB Front Side	
31 SATA Connector	
32 HDMI Connector	
34 ACPI uPI-5VDIMM&3VSB	
35 PM-SY8288RAC-1.05V/GS7133-2.5V	
36 DDR PWR VPP25/VTM-MP2147	
37 DDR Power-RT8231AGQW	

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Schematic Cfg		Project	
		V	A

MSI		MICRO-START INT'L CO.,LTD.			
Title					
AM4 DDR4 I/F					
Size	Document Number	Rev			
Custom	MS-7B87	11			
Date	Monday, June 25, 2018	Sheet	3 of 56		

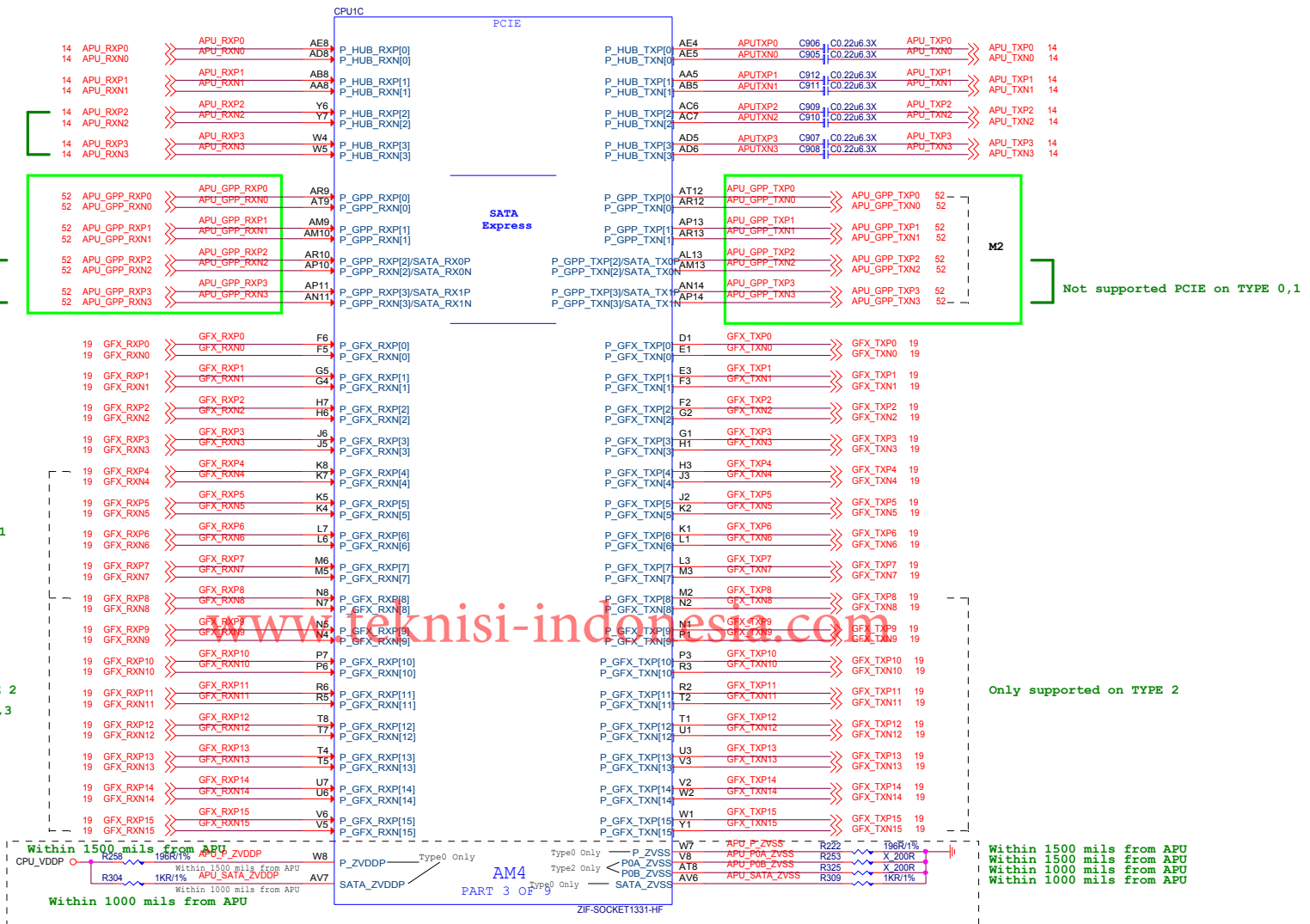
Not supported HUB on TYPE 1

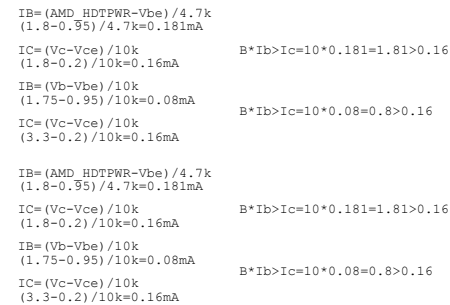
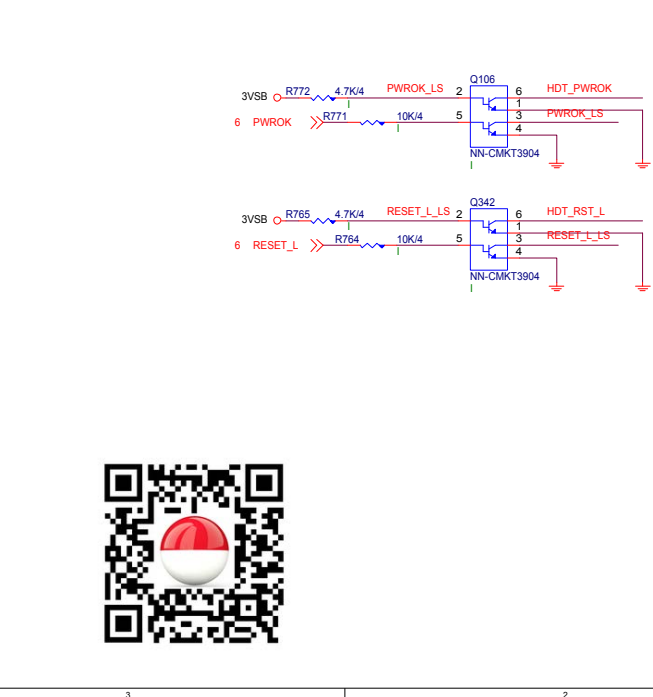
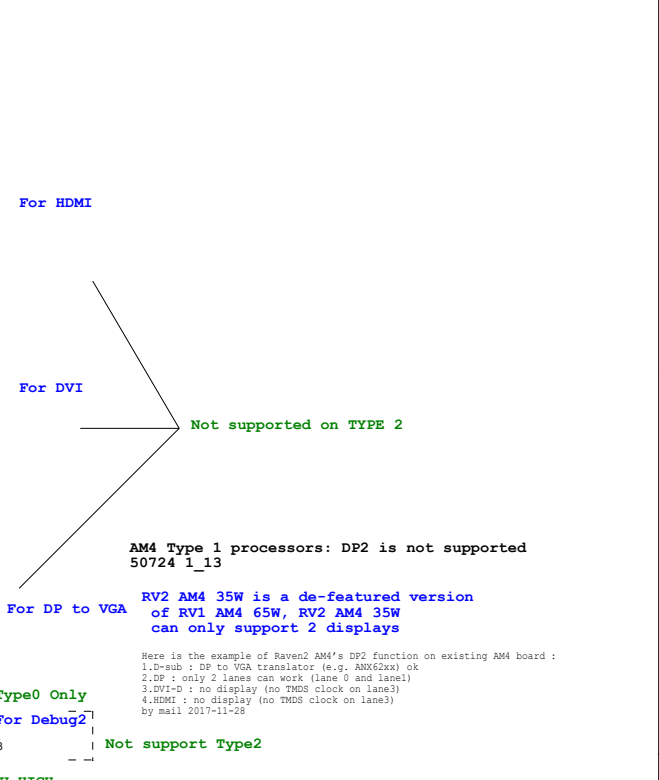
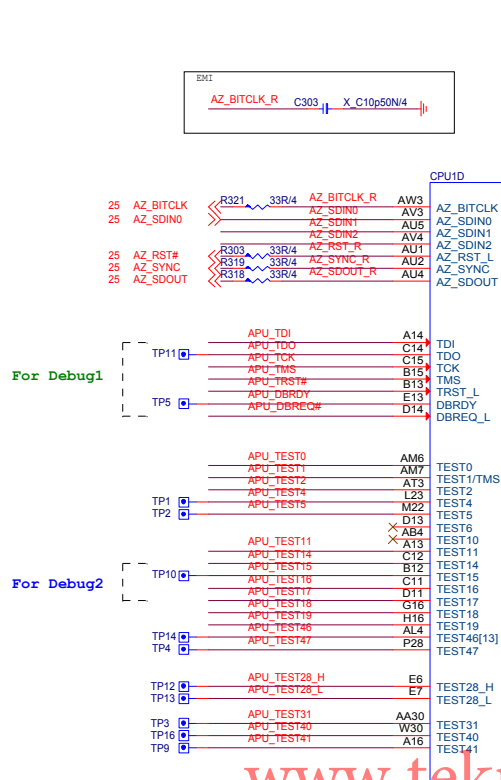
Not supported PCIE on TYPE 0,1

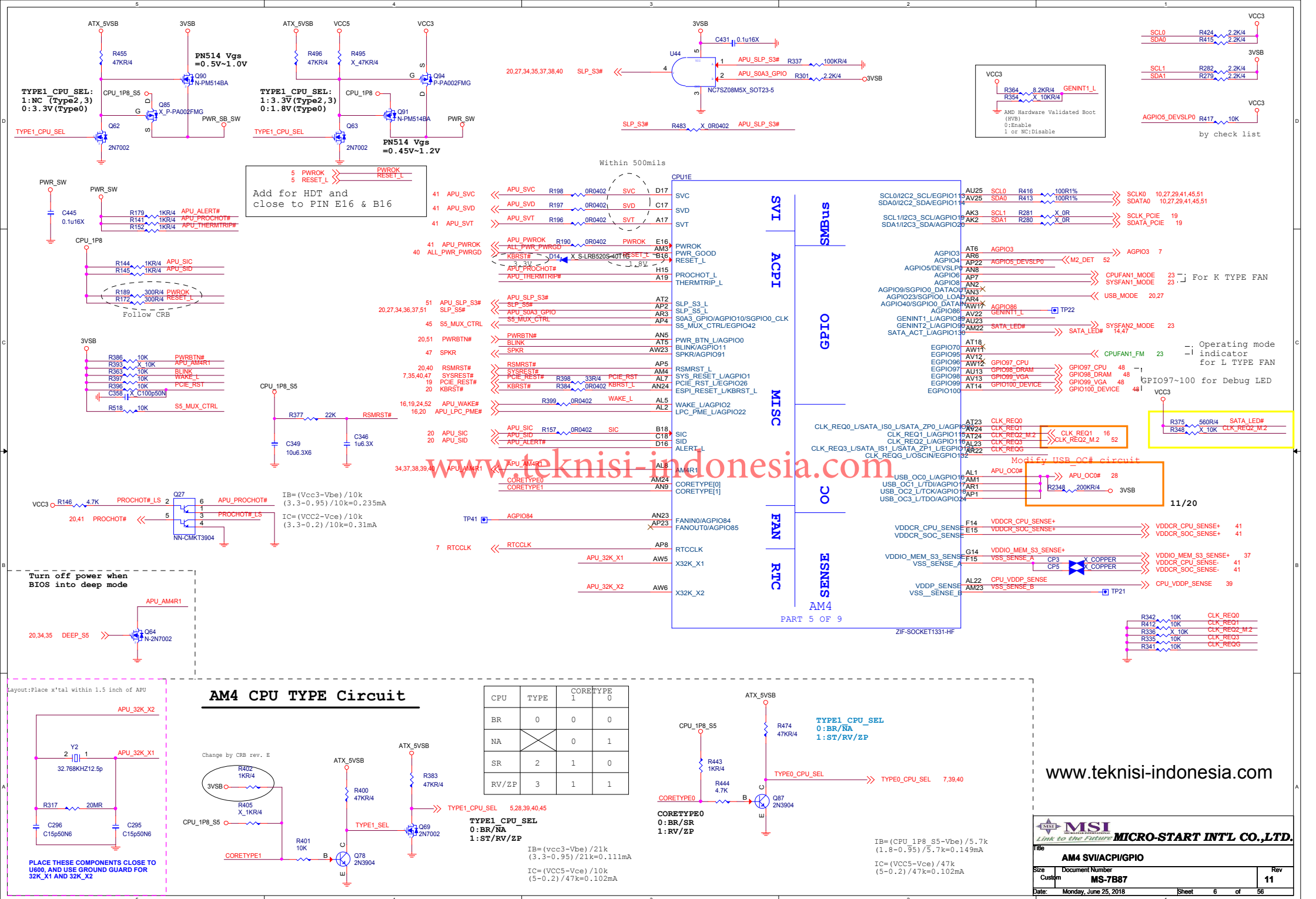
TYPE	PCIE	SATA
TYPE 0	2	2
TYPE 2/3	2 or 4	2 or 0

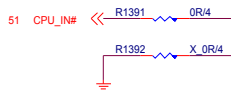
Not supported GFX 4~15 on TYPE,1

Only supported on TYPE 2
Not supported GFX 8~15 on TYPE 0,3









A1



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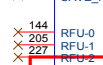
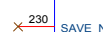
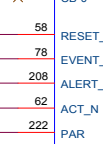
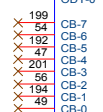
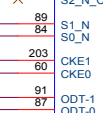
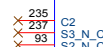
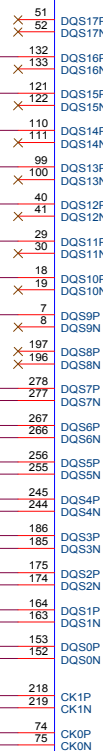
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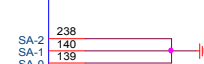
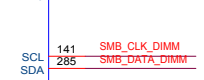
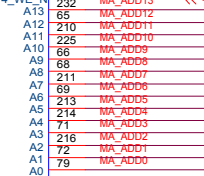
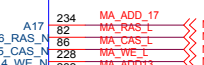
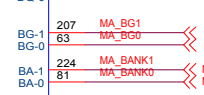
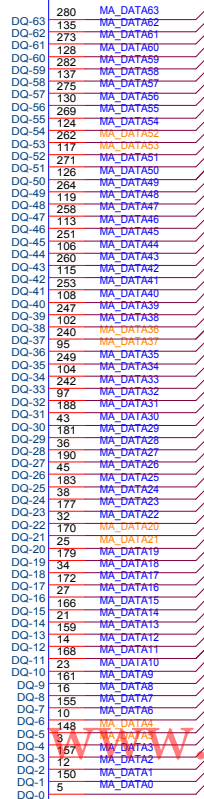
A

DIMMA1A



DDRIV-288P_RED-RH

轉正式Footprint

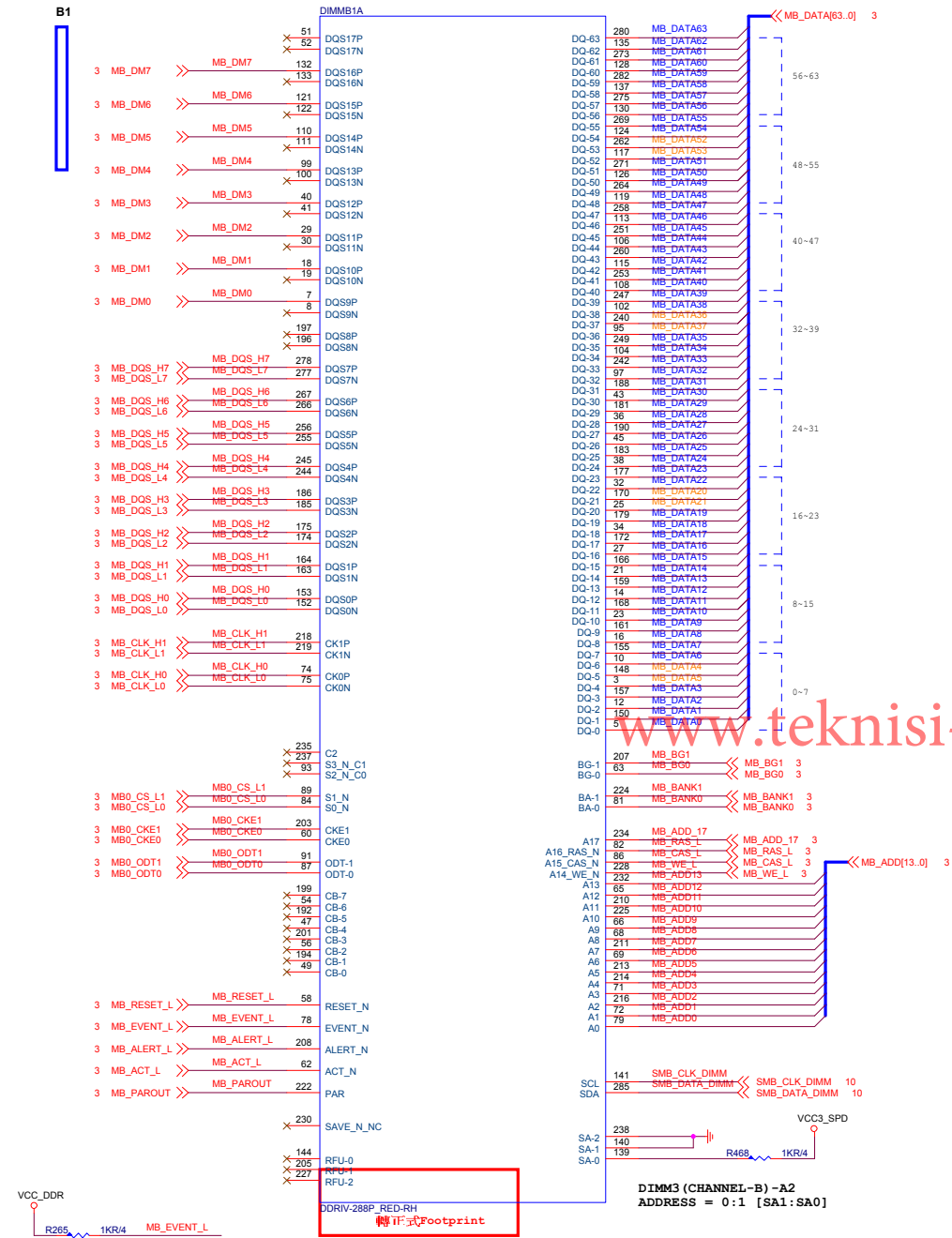


DIMM1 (CHANNEL-A) -A0
ADDRESS = 0:0 [SA1:SA0]



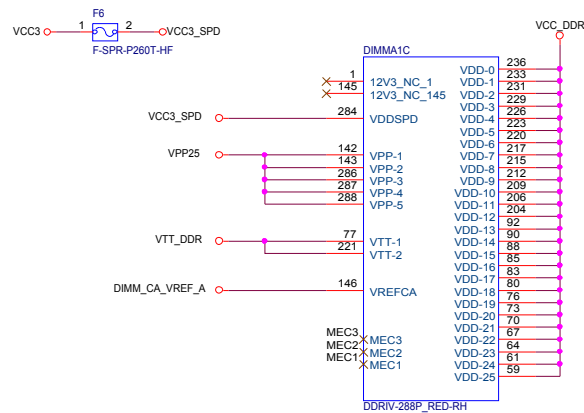
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DDR4 DIMM CH-A
Document Number MS-7B87
Rev 11
Date: Monday, June 25, 2018 Sheet 10 of 56

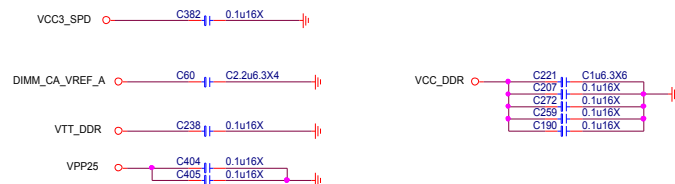


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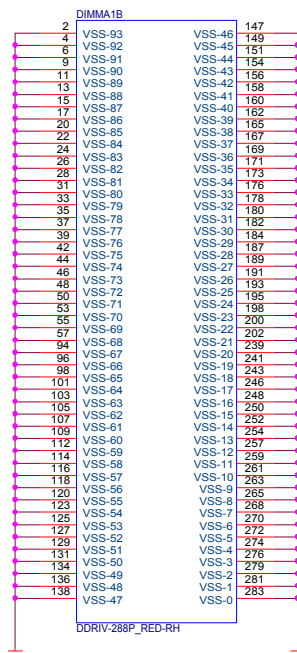




DIMM SLOT PN BY SPEC

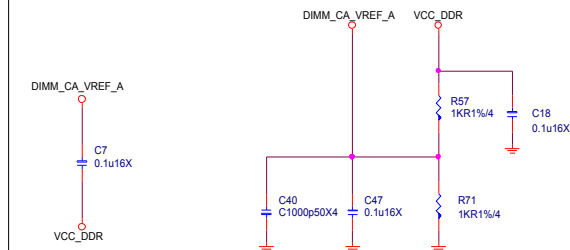


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DDR VREF

(place resistors close to DIMMs)

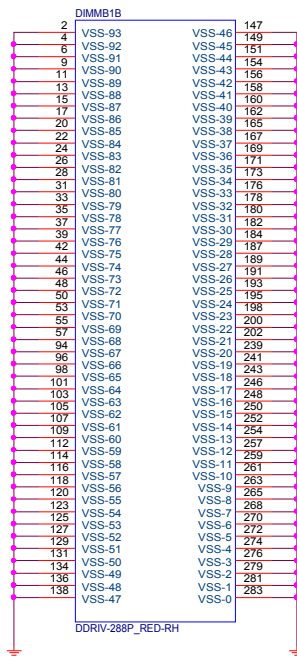
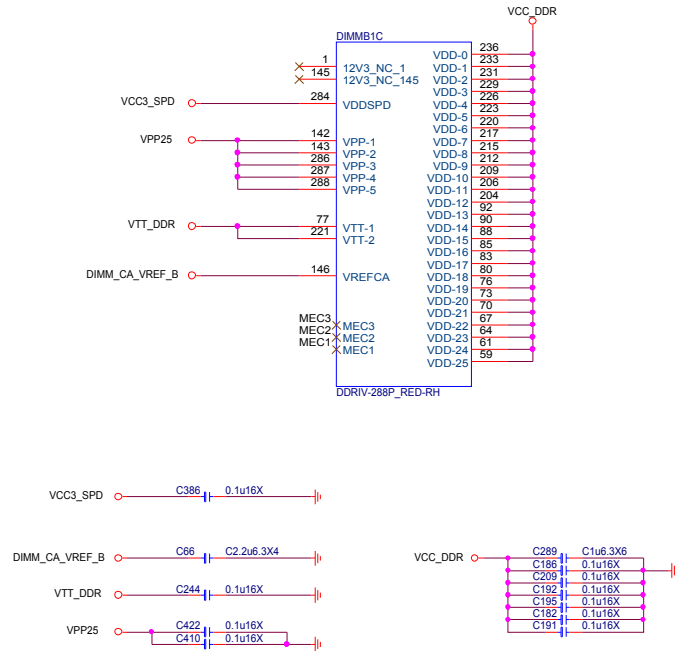
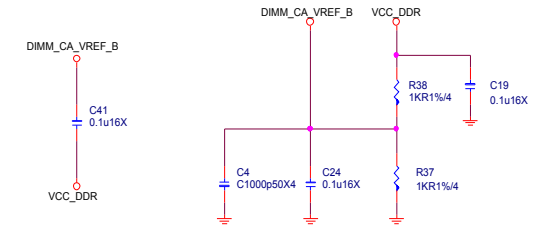


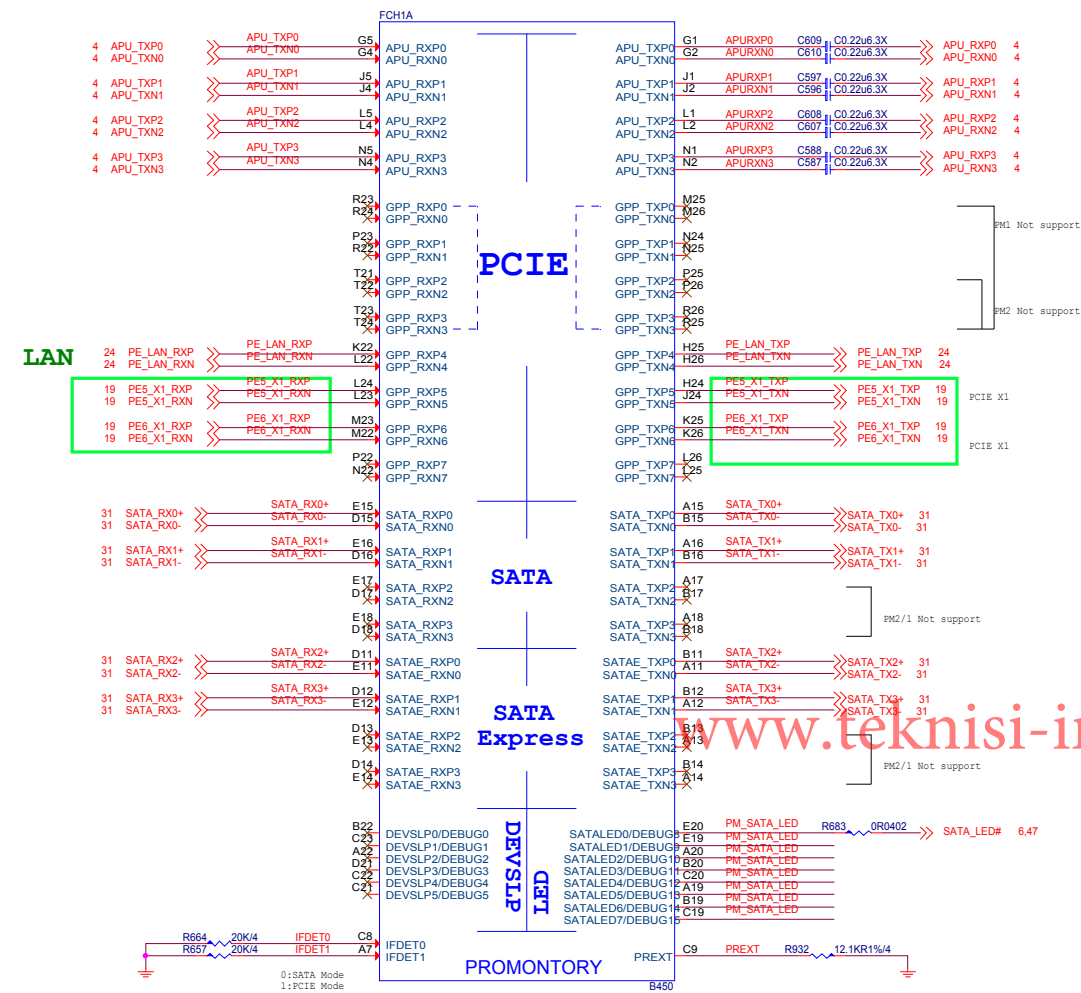
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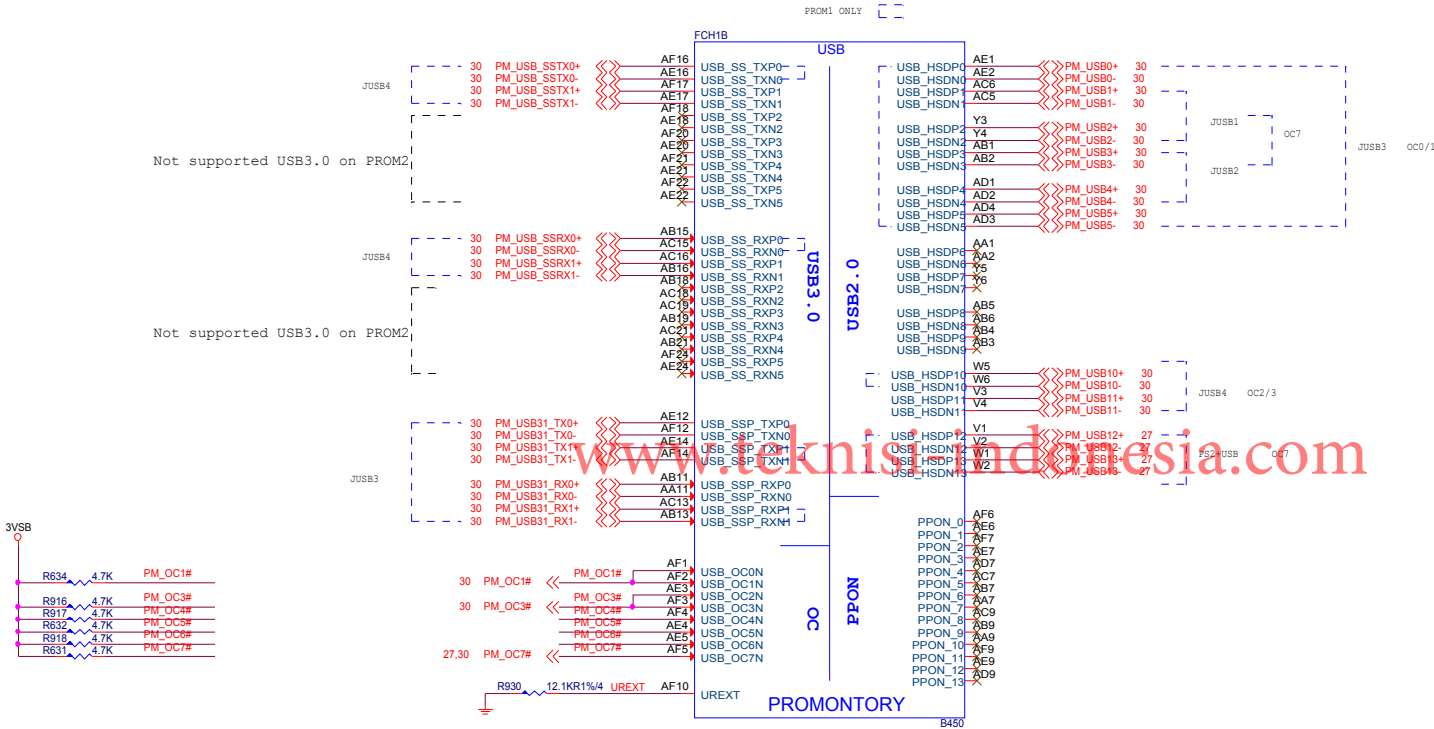
DDR VREF

(place resistors close to DIMMs)





SATA Express port0 (IFDET0)
SATA Express port1 (IFDET1)
0:SATA Mode
1:PCIE Mode



Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

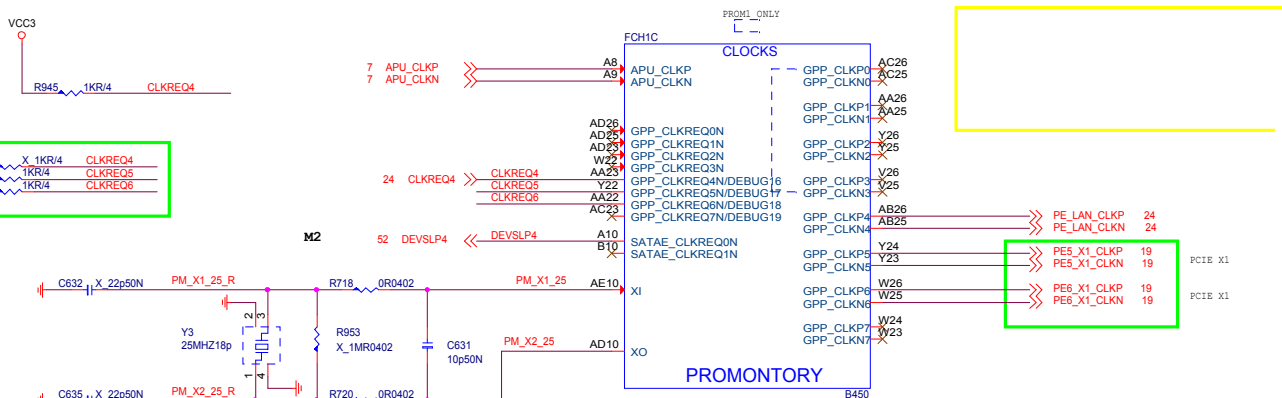
Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~3	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

CLK2.3不能用
CLK1-3不能用

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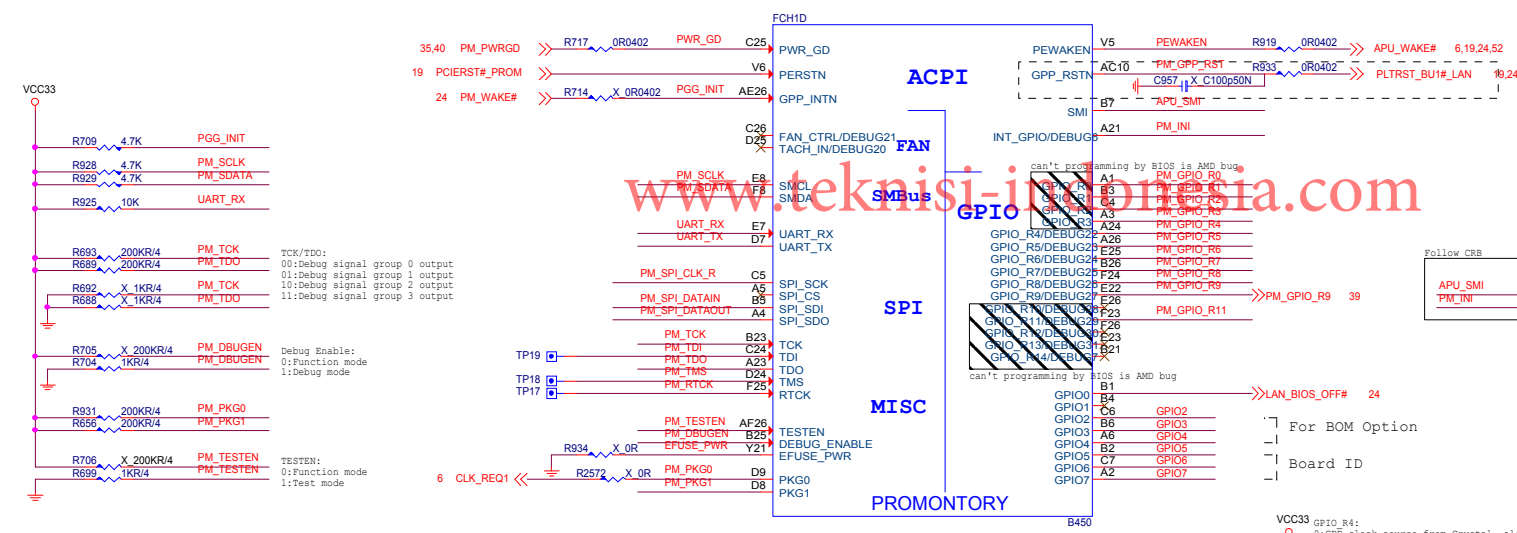


Appendix C Port Mapping for Different Bus Models

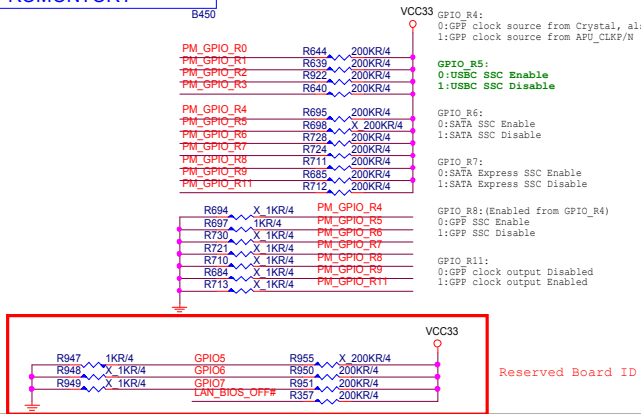
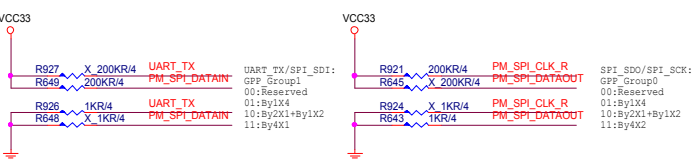
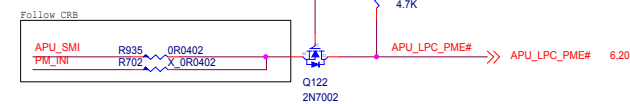
BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~3	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

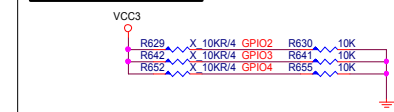
CLK2.3不能用
CLK1-3不能用



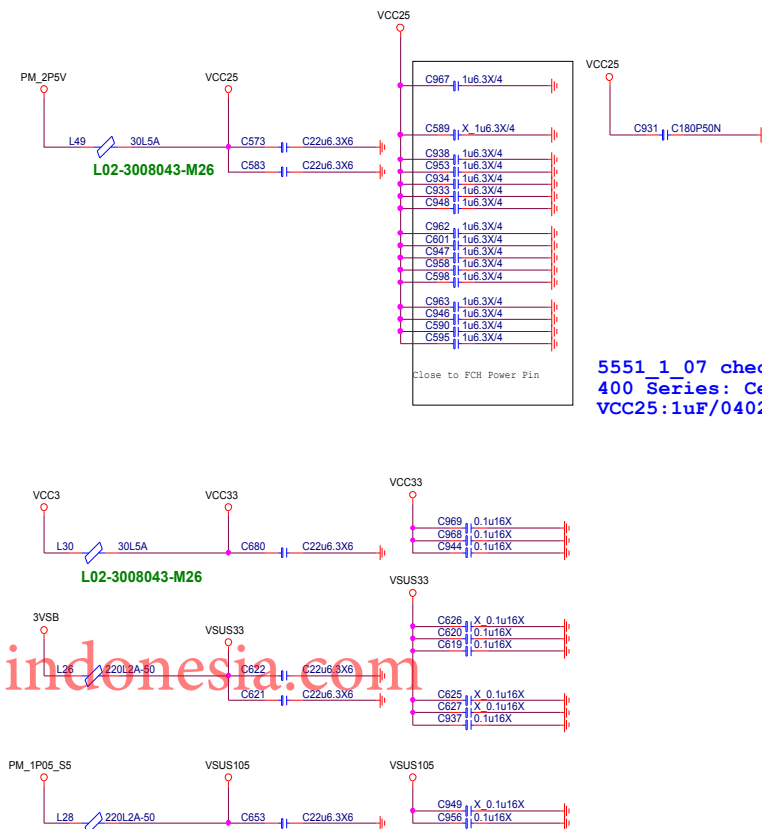
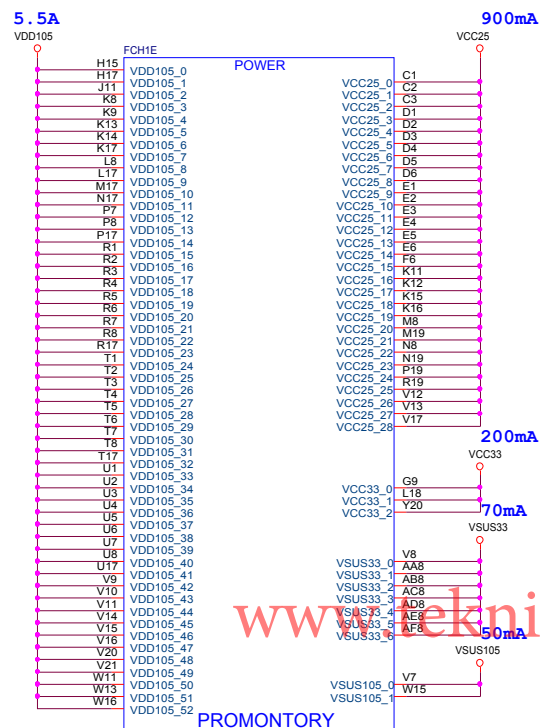
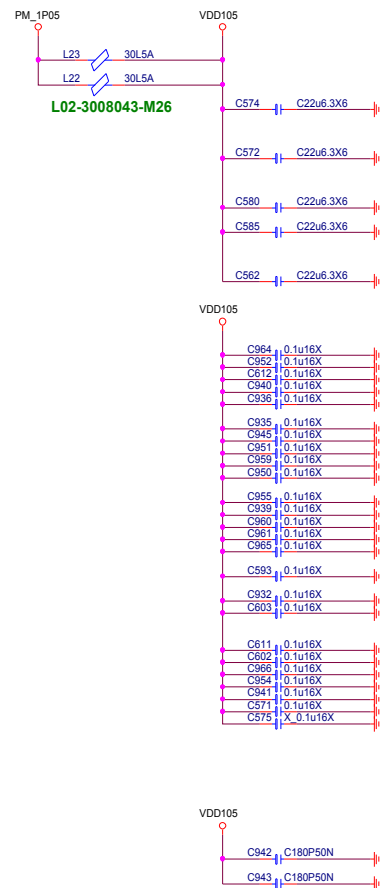
Co-layer GPP_RSTN Reset for meet FCH sequence. See 55553.



BOM OPTION



	FULL	
GPIO2	0	
GPIO3	0	
GPIO4	0	



5551_1_07 check list
400 Series: Ceramic capacitors.
VCC25:1uF/0402

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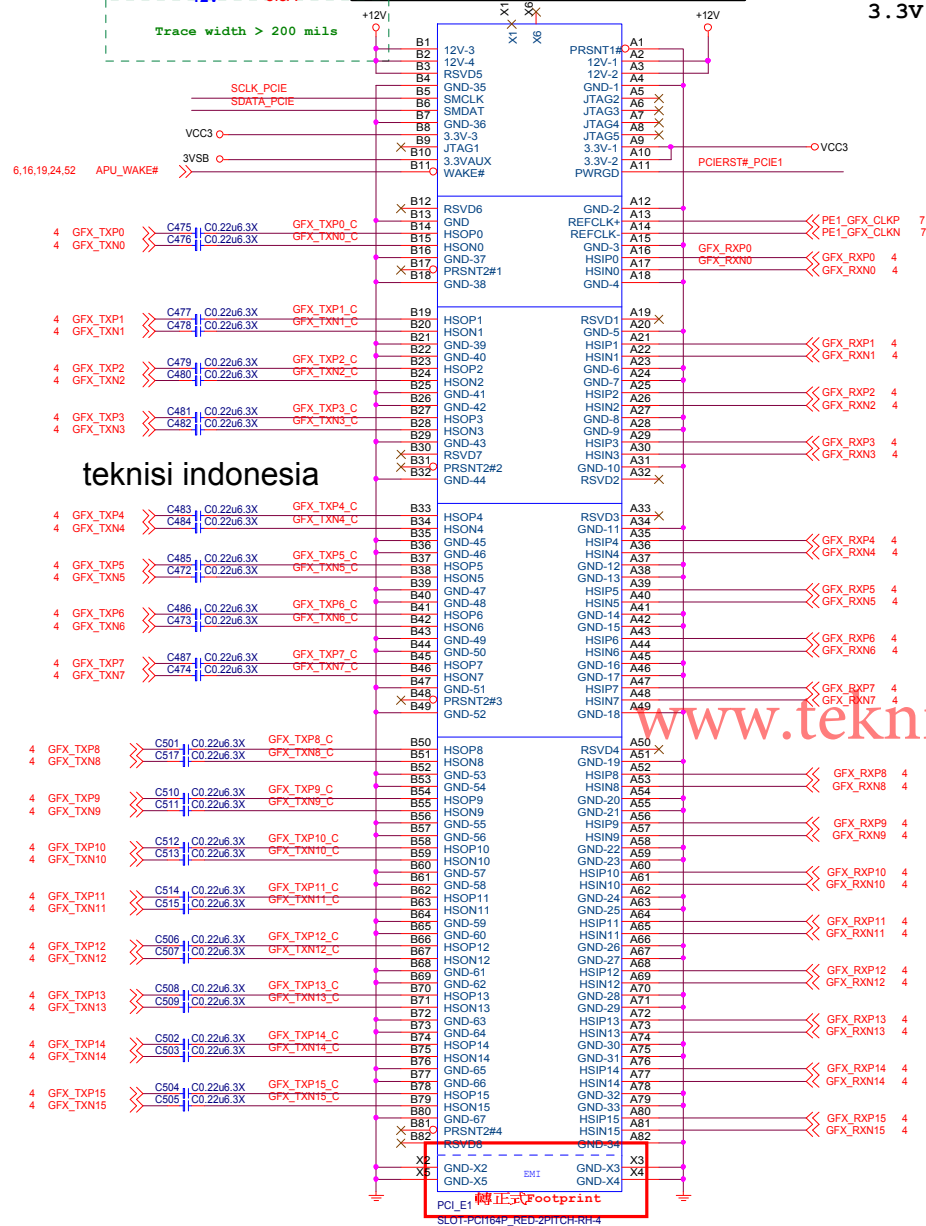
GND

PROMONTORY

8450

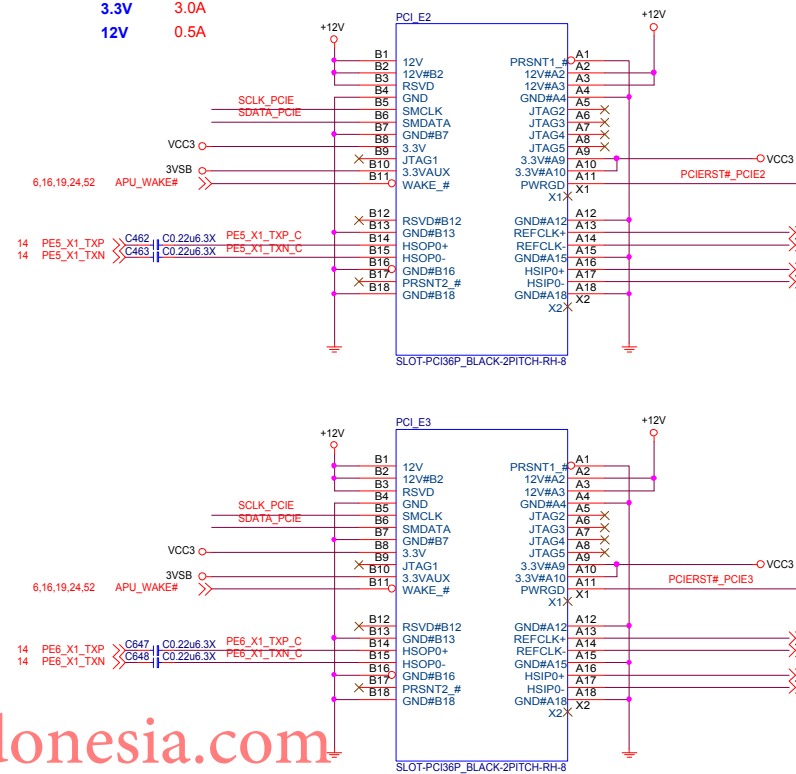
3.3V 3.0A
12V 5.5A

PCI EXPRESS x16 Slot

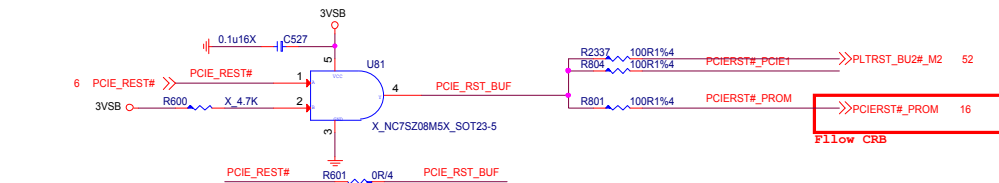
PCIEX1 12V 0.5A
3.3V weak 375mA

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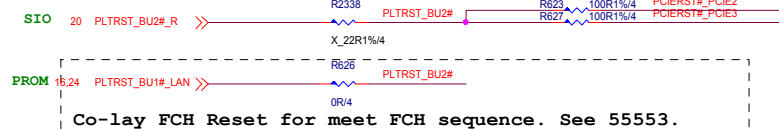
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3.3V 3.0A
12V 0.5A

within 500mil

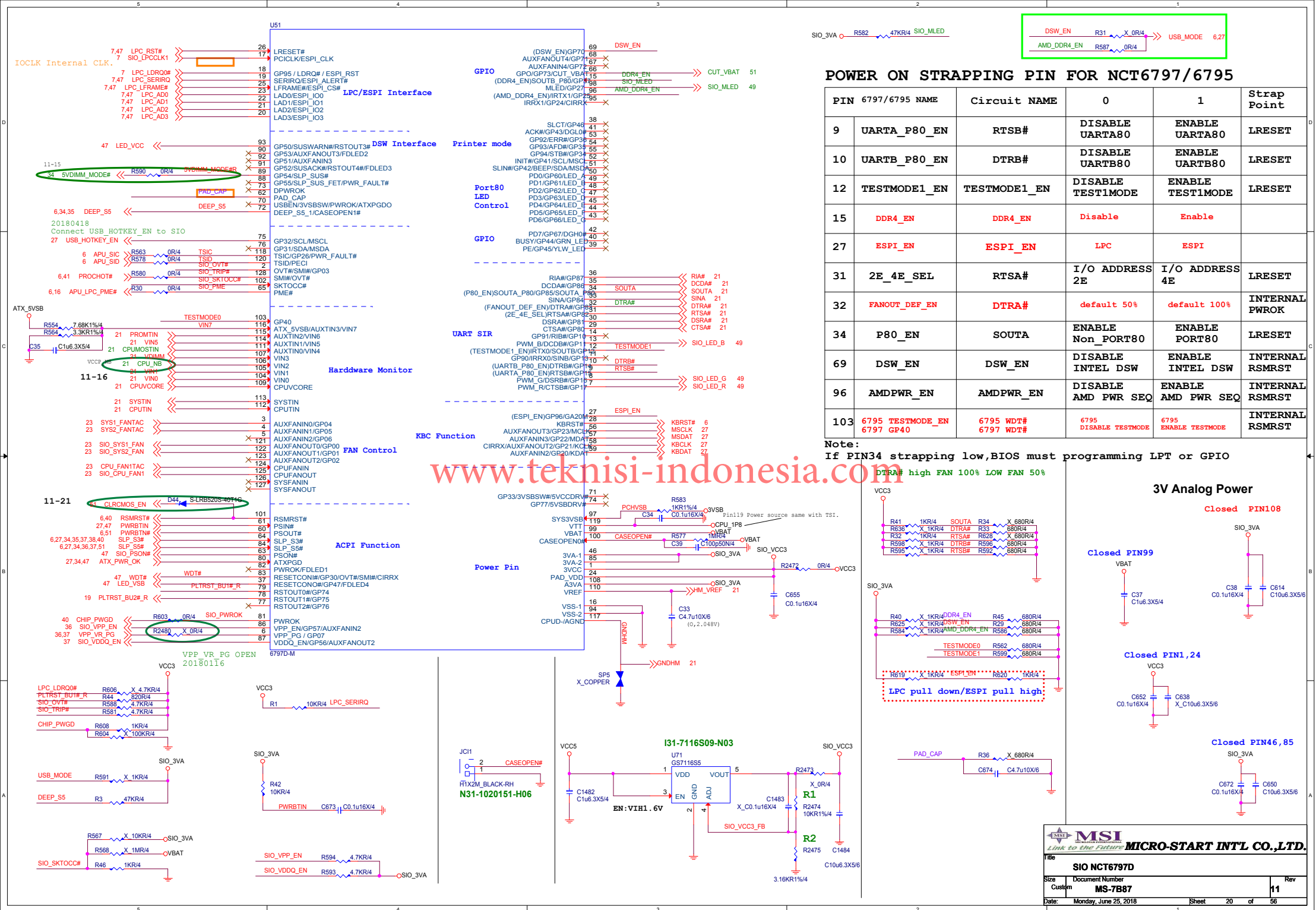


PROM RESET

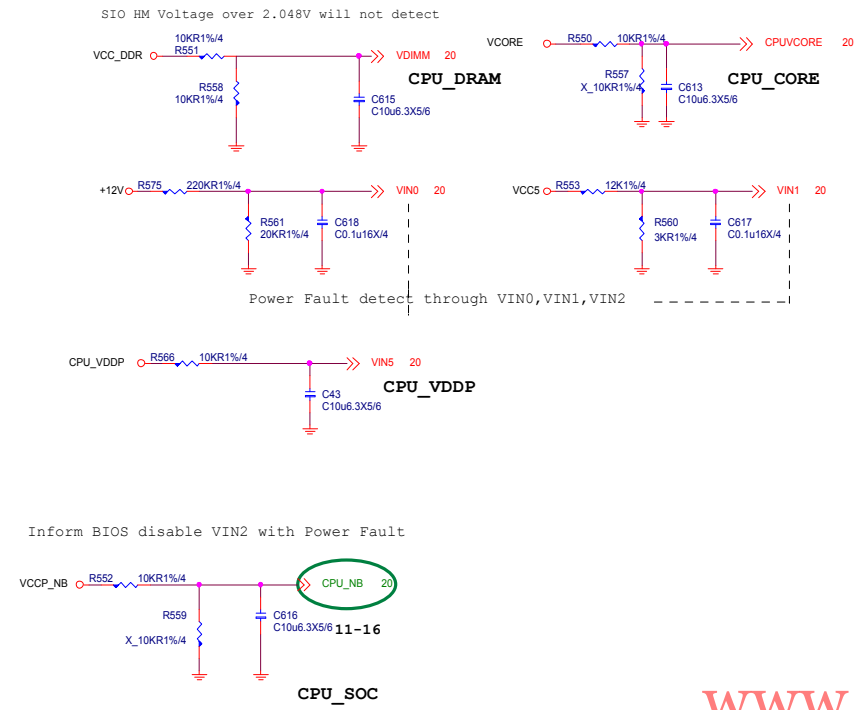


SMBus separate circuit

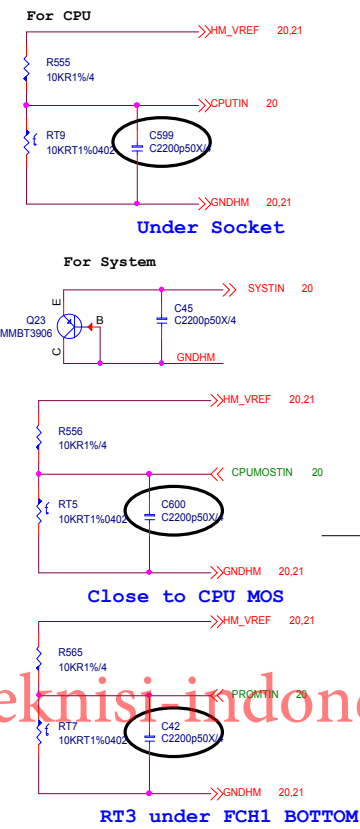




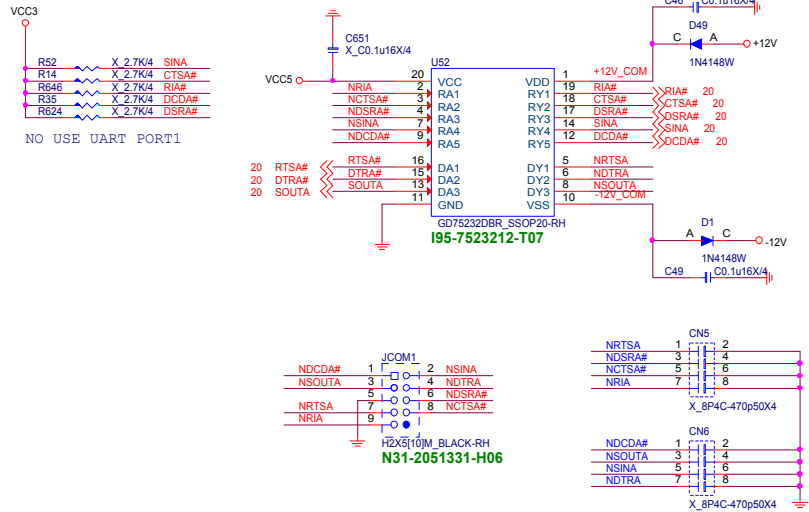
HW Monitor - Voltage



TEMP SENSOR



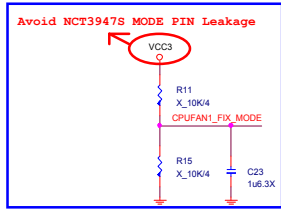
COM PORT



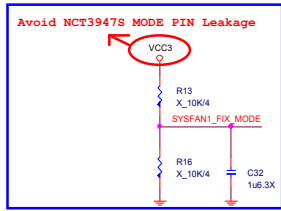
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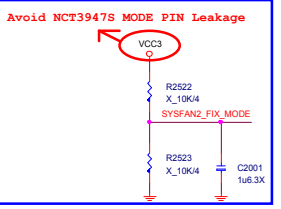
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE
2.GPIO可以由BIOS切换 PWM/DC MODE



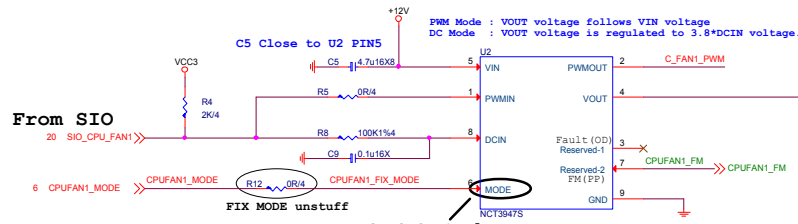
Resever For FIX DC or PWM MODE USE By PM SPEC



Resever For FIX DC or PWM MODE USE By PM SPEC

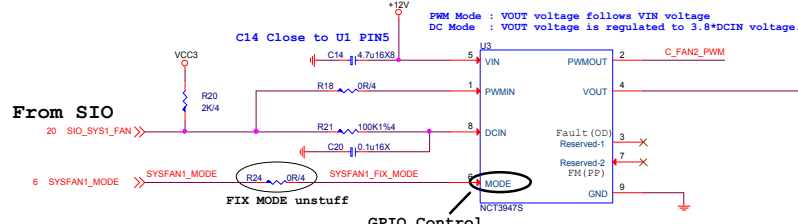
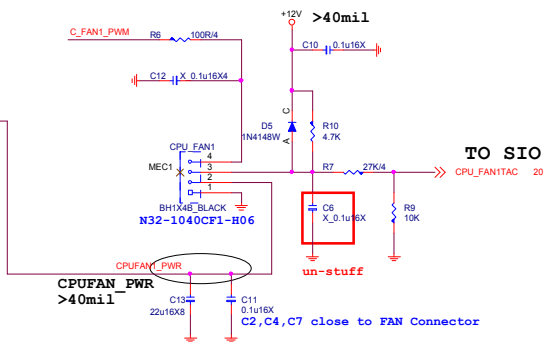


Resever For FIX DC or PWM MODE USE By PM SPEC



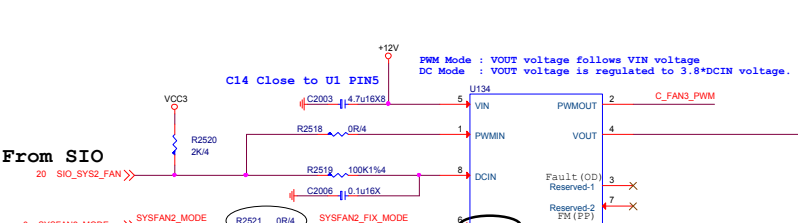
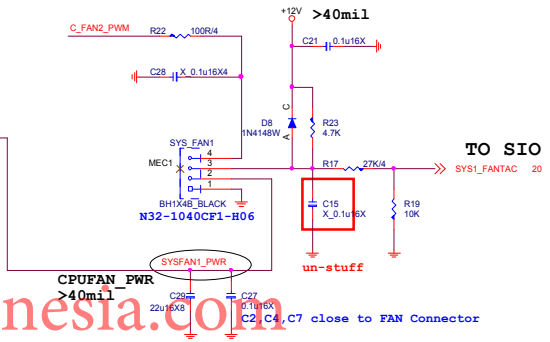
GPIO Control	
	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



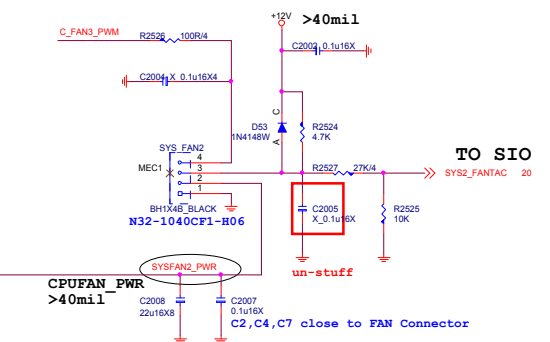
GPIO Control	
	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

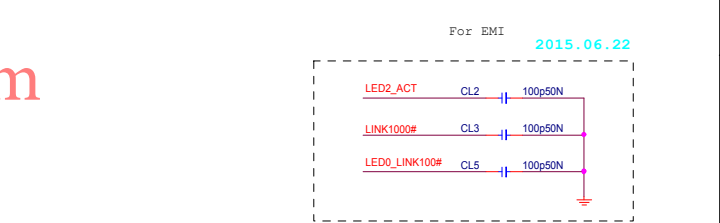
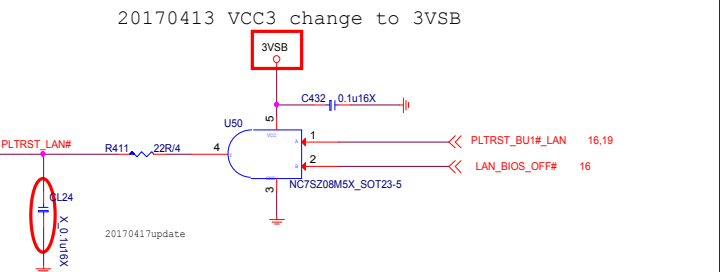
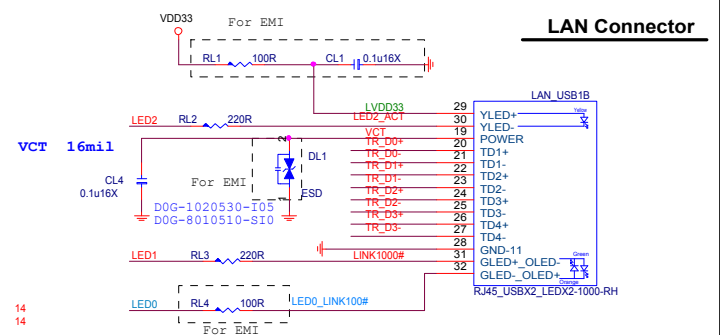
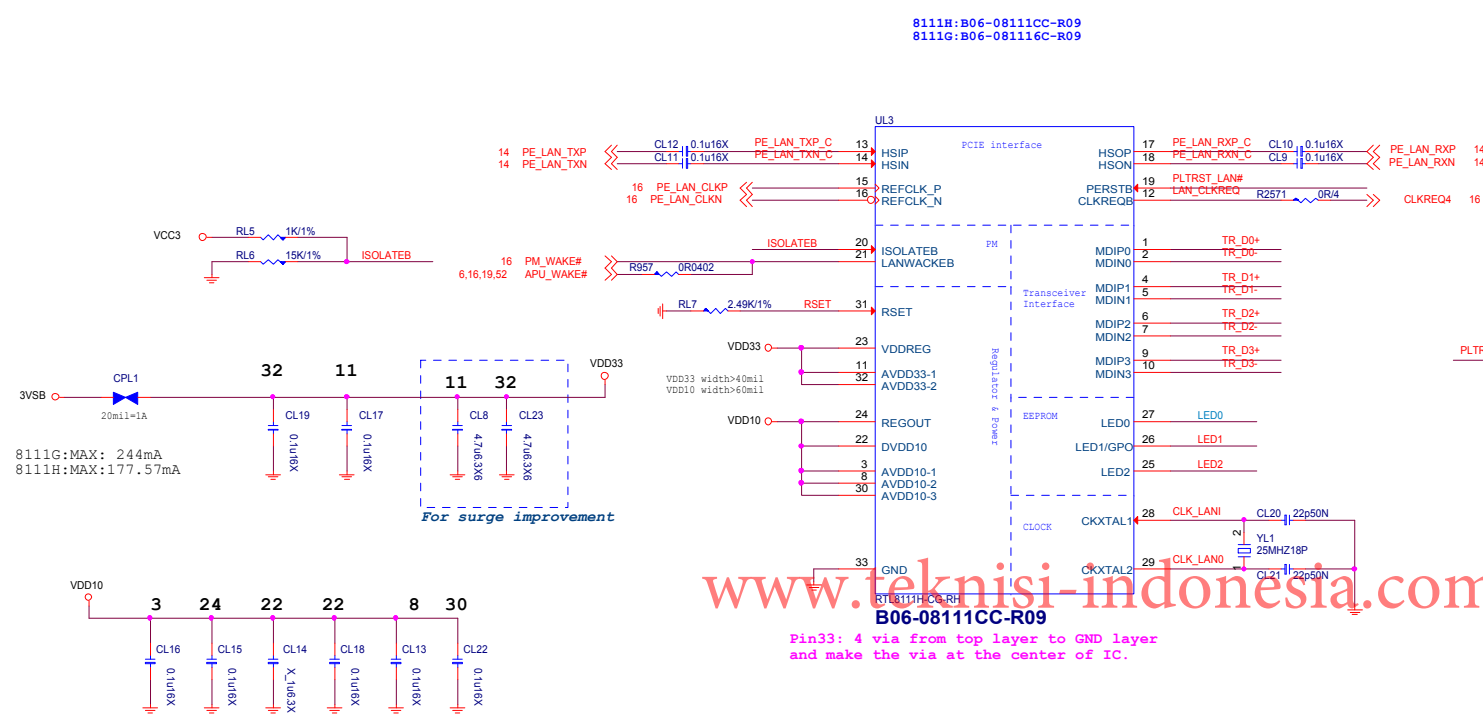


GPIO Control	
	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



RTL8111G/RTL8111H Giga LAN



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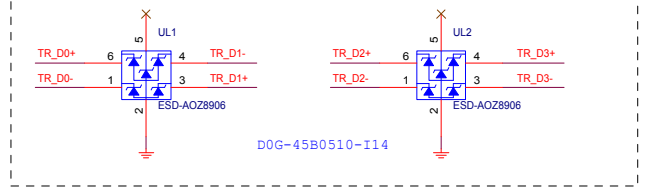
8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

ESD Protect
UL2&UL3 close to connector



MSI MICRO-START INTL CO.,LTD.

LAN-RTL8111H

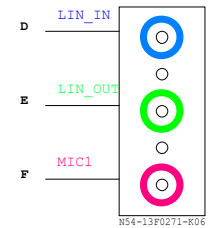
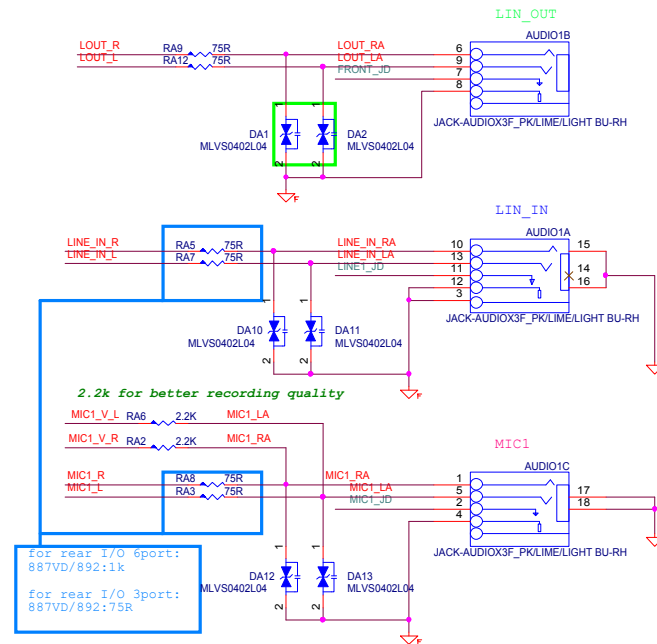
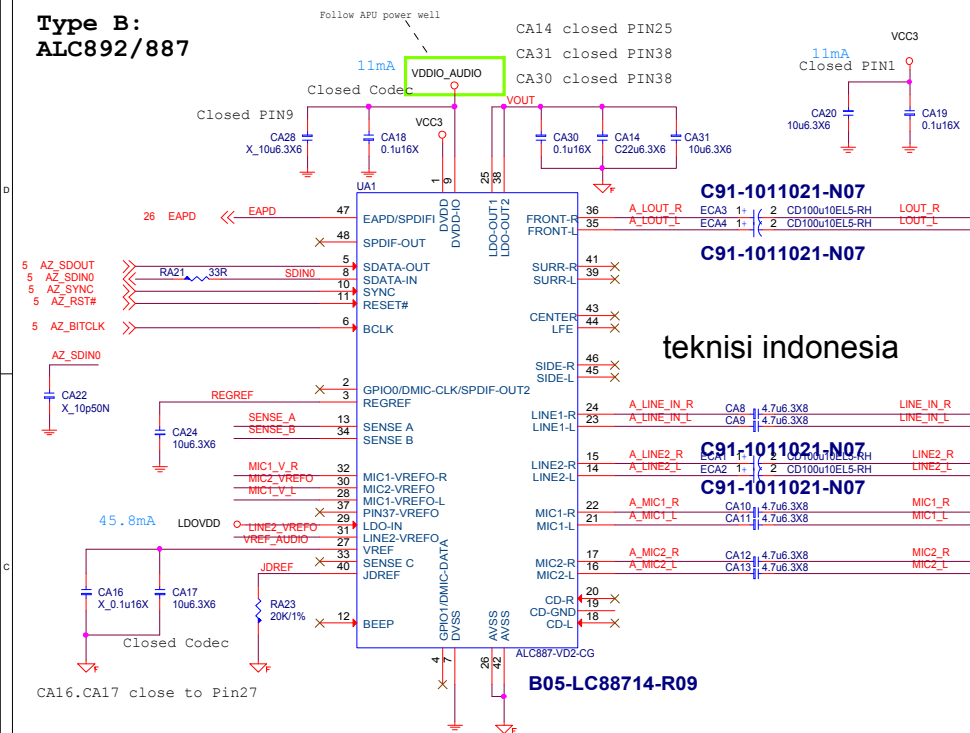
Document Number MS-7B87

Date: Monday, June 25, 2018

Sheet 24 of 56

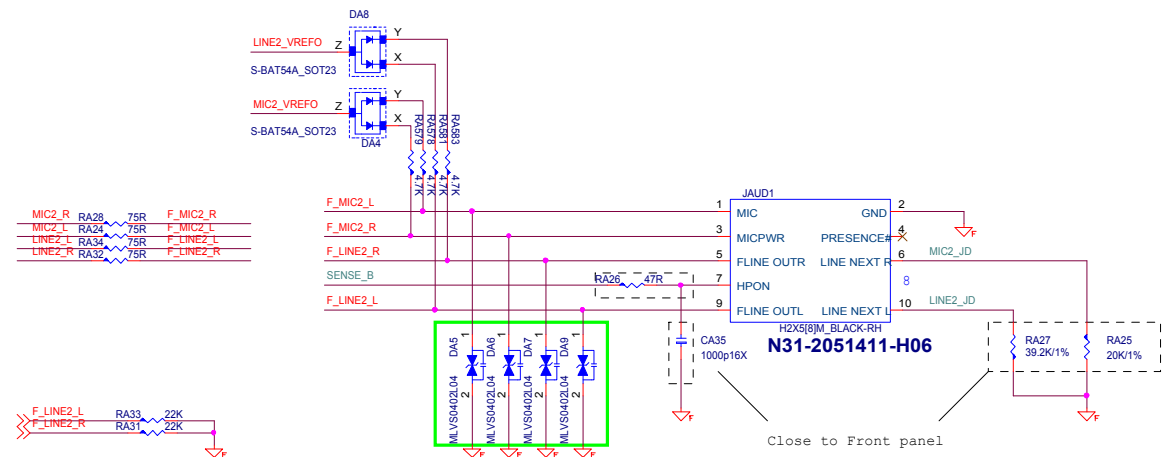
Rev 11

Type B:
ALC892/887



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Varister --> cap for cost down

D0G-2710510-I05
D0G-2950500-SI0

Close to Jack

Close to Front panel
For HDA/AC97 front cable.



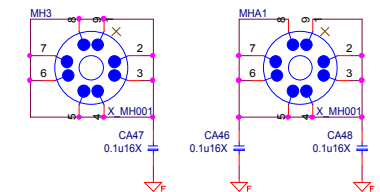
Title	Audio ALC887-1
-------	----------------

Size	Document Number	Rev
Custom	MS-7B87	11

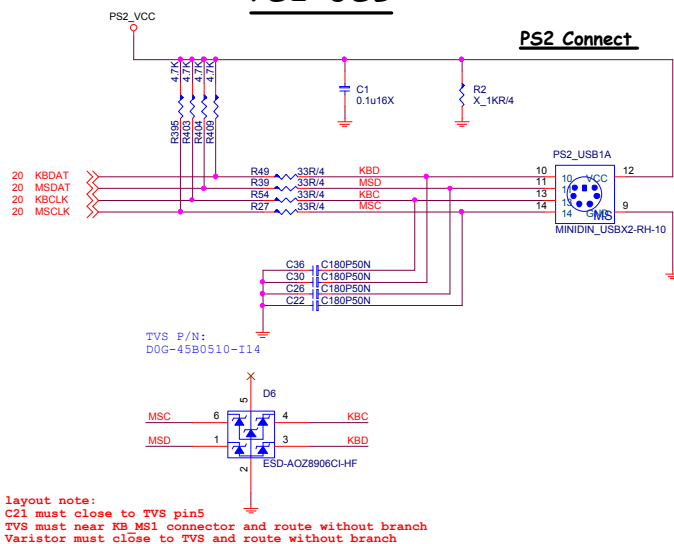
De-pop circuit for Rear Line out & Front Headphone out)



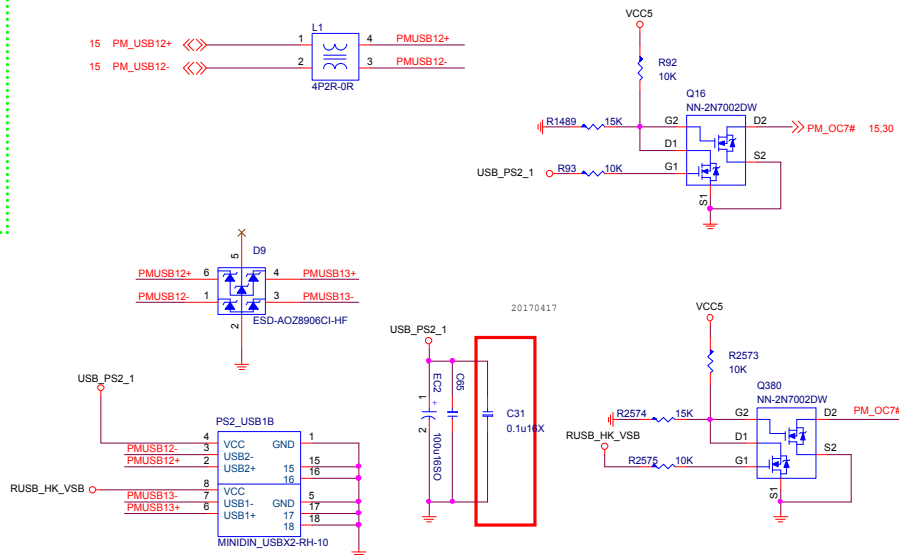
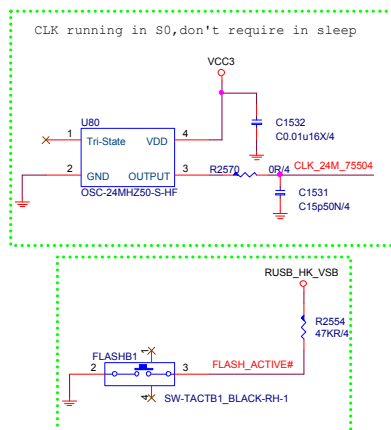
Analog



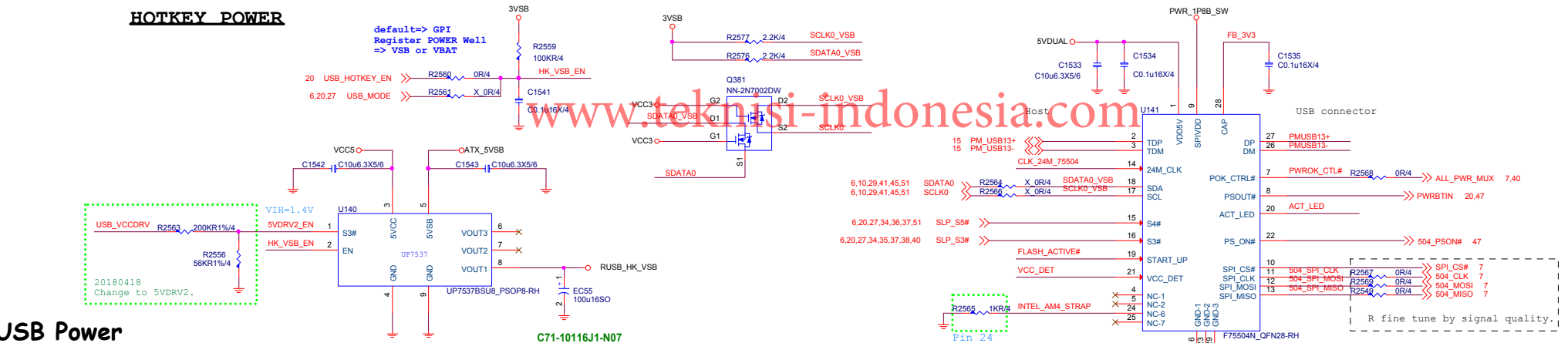
PS2+USB



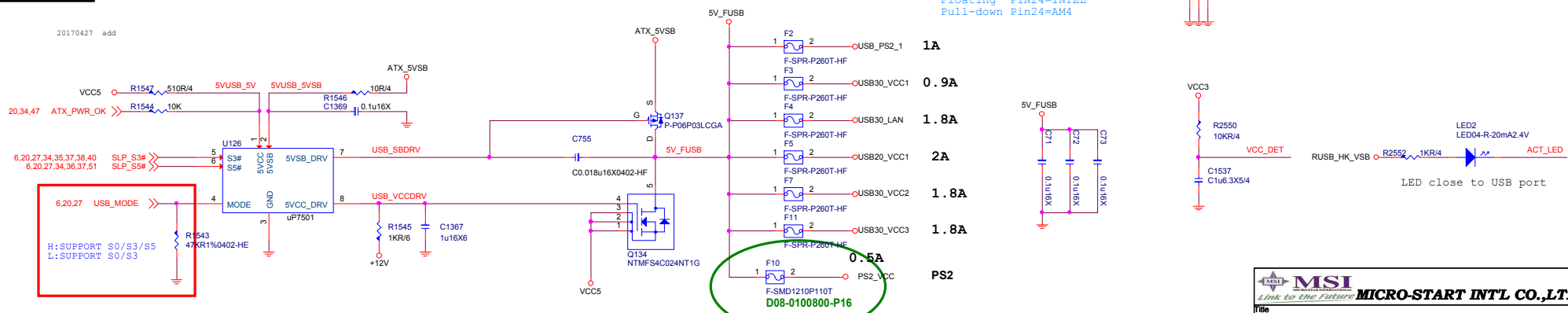
layout note:
C21 must close to TVS pin5
TVS must near KB_MSI connector and route without branch
Varistor must close to TVS and route without branch



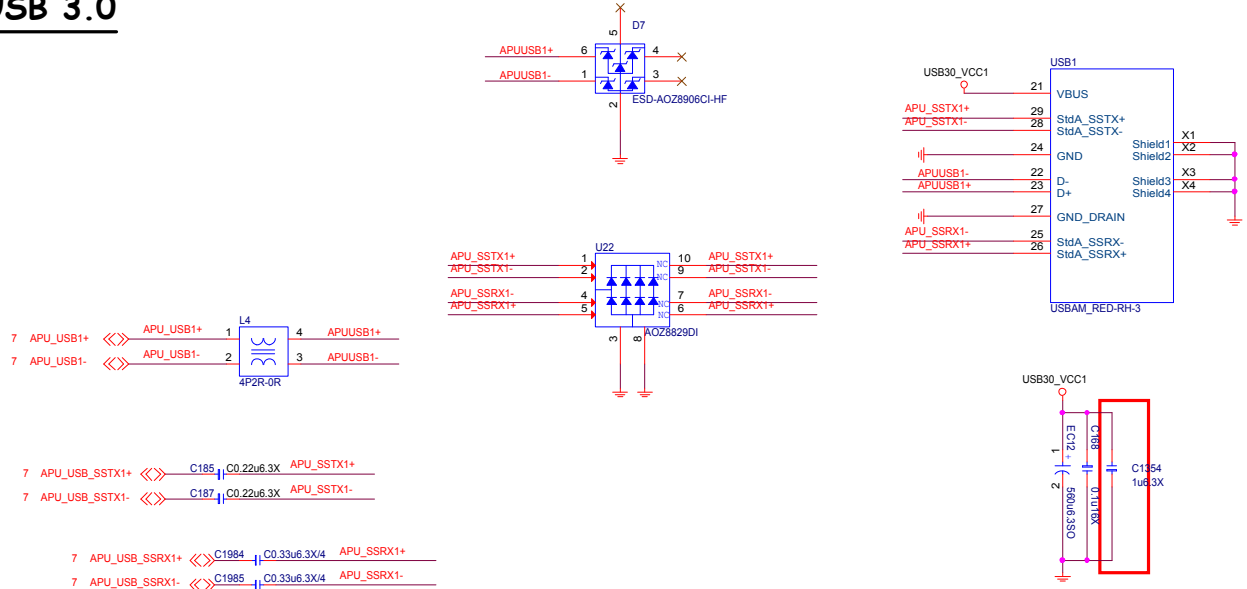
HOTKEY POWER



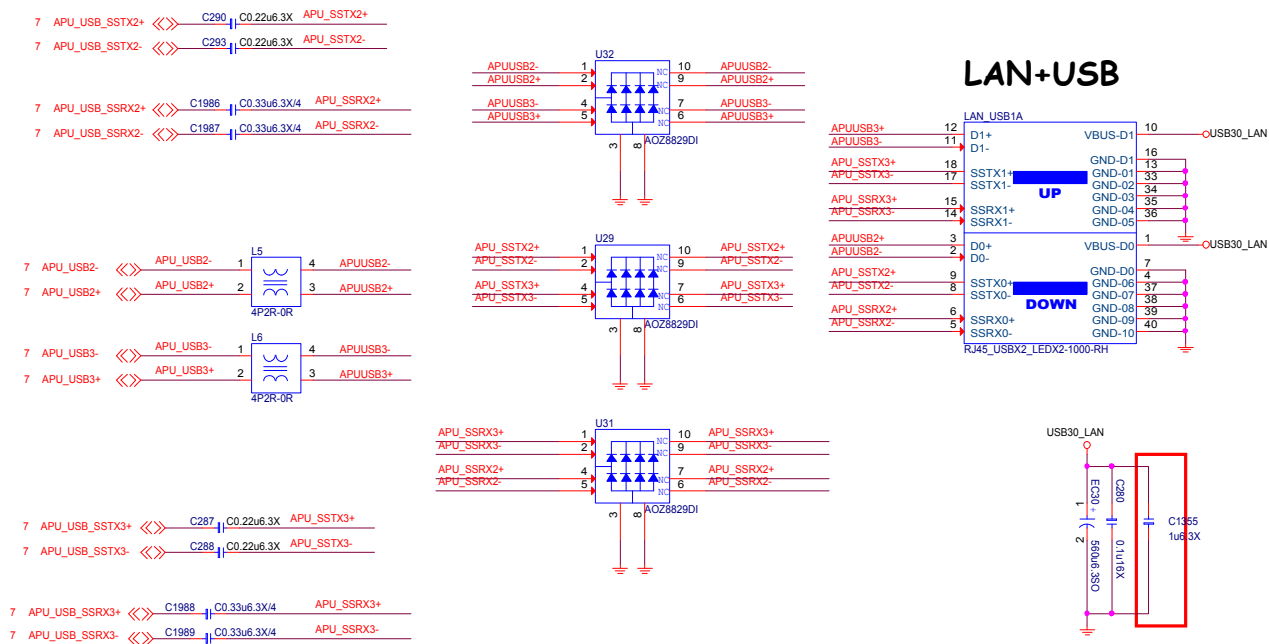
USB Power



USB 3.0

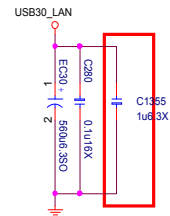


USB3.1 GEN1

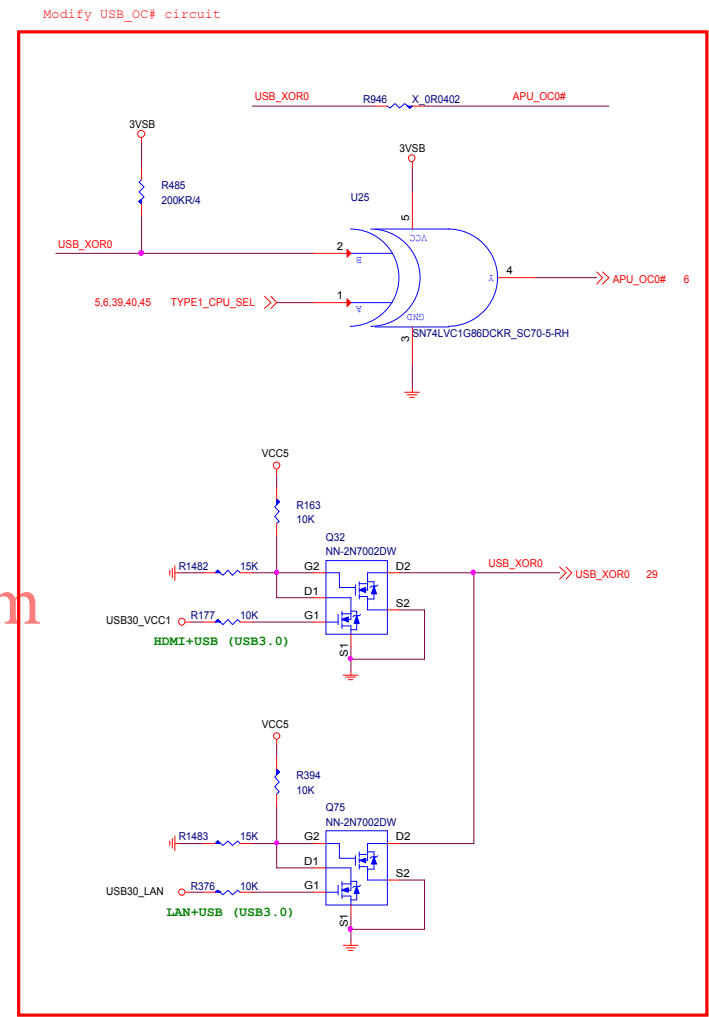


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LAN+USB

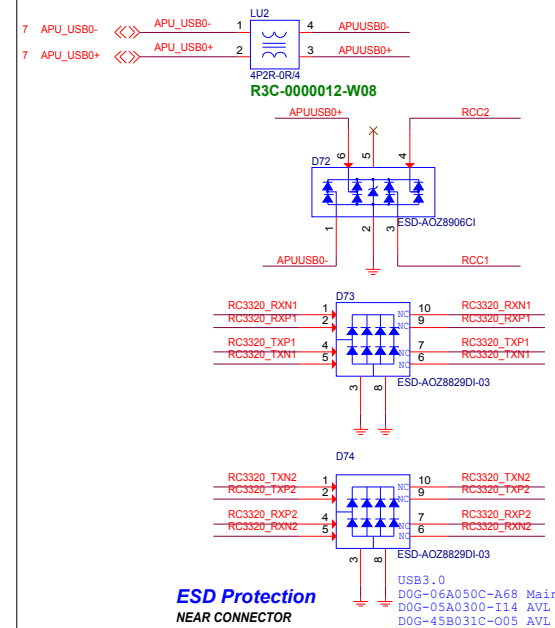
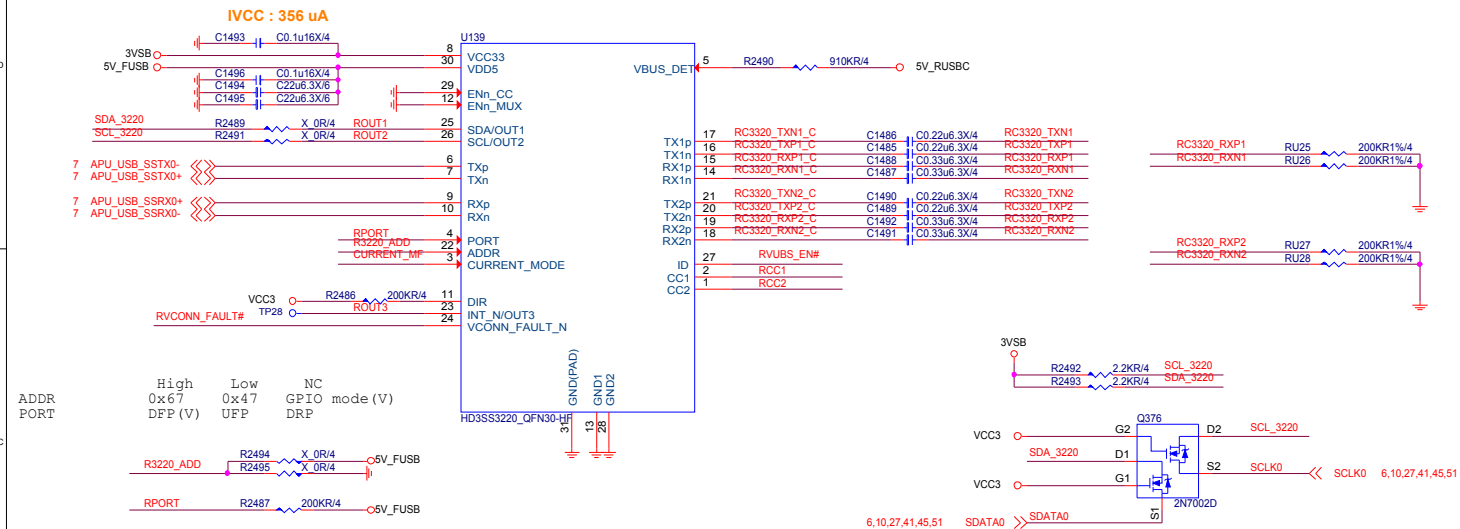


APU_USB_OC

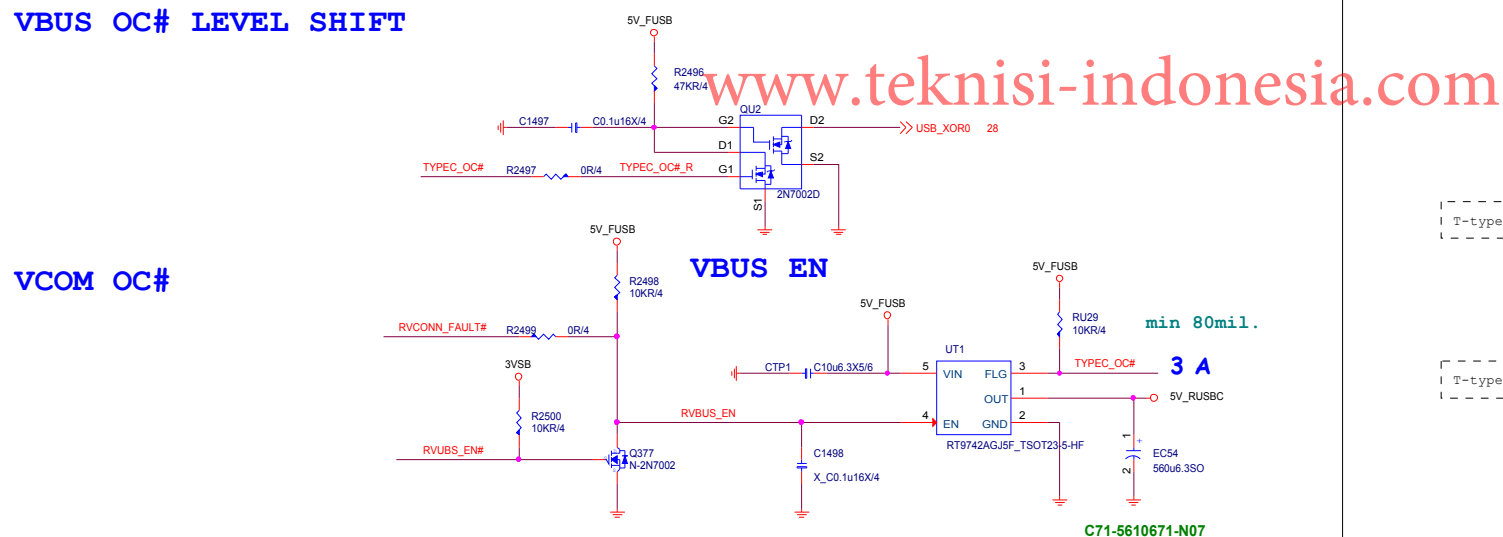


	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

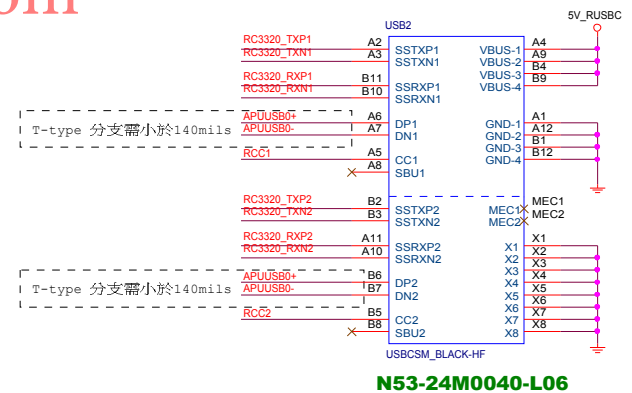
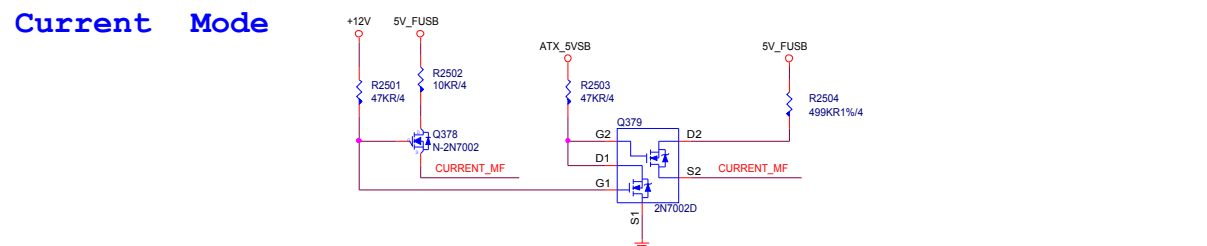
USB 3.1-Type-C USB Type-C MUX with Configuration Channel (CC)



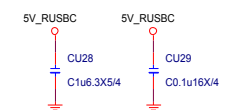
VBUS OC# LEVEL SHIFT



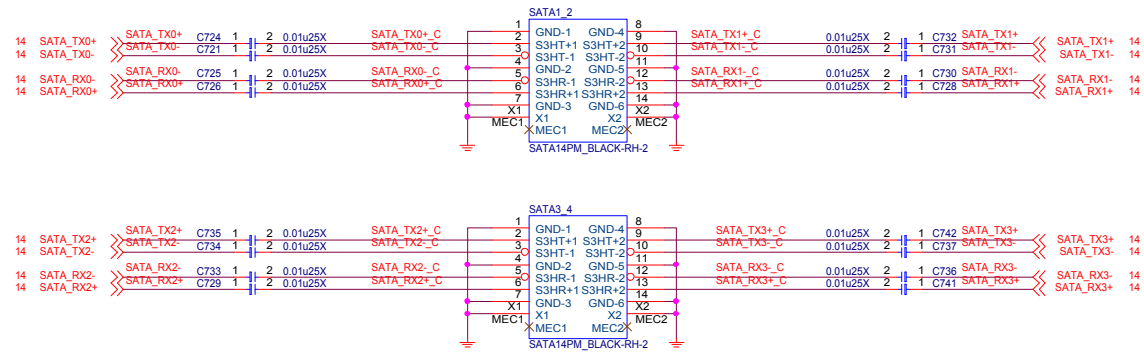
Current Mode



close to Type C Connector



SATA Connector

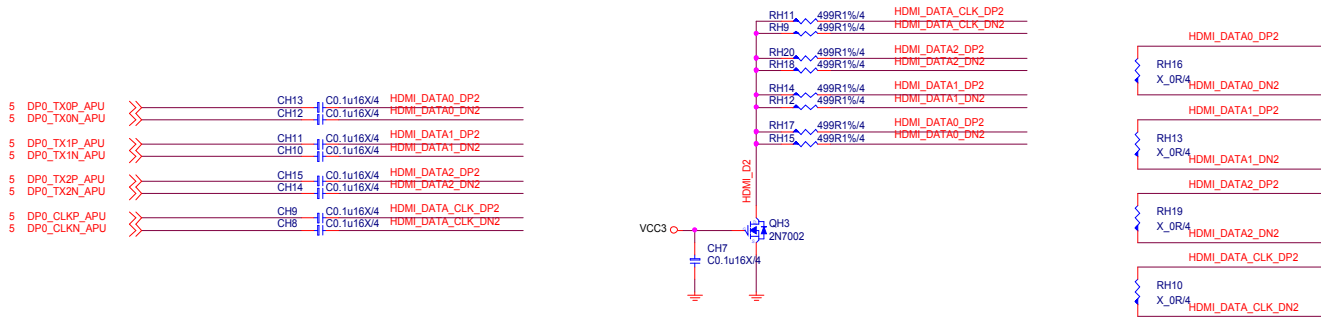


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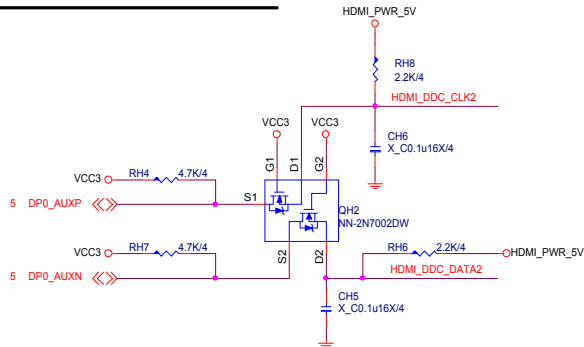
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HDMI CONNECTOR

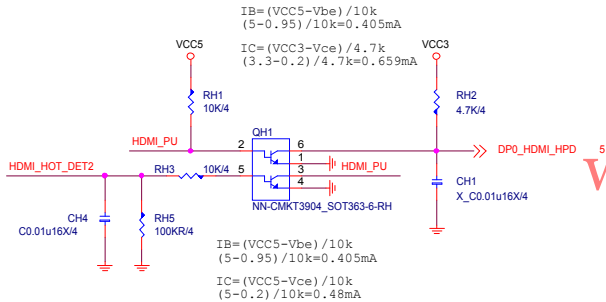
For HDMI 1.4



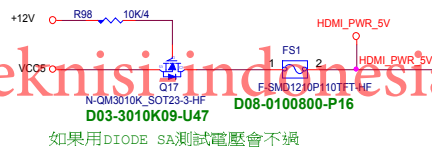
AUX Level Shifter



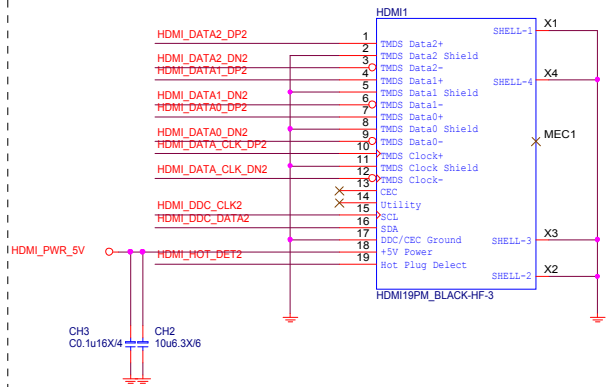
HPD Circuit



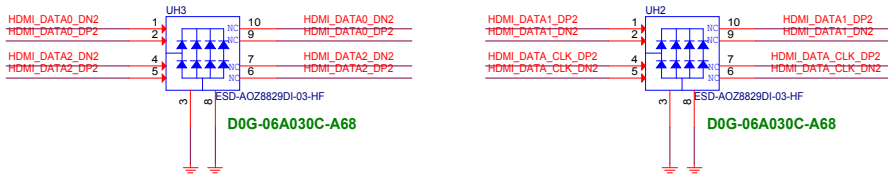
Connector Power



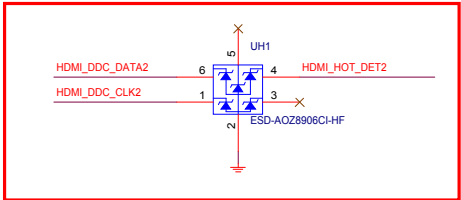
Connector




For EMI



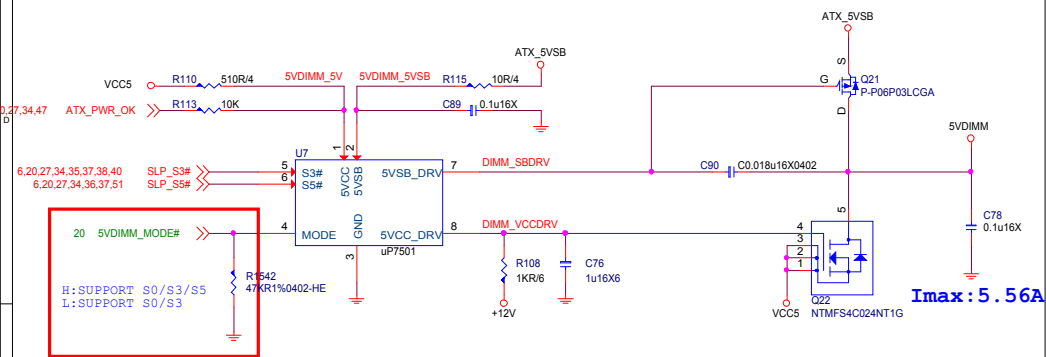
20170426



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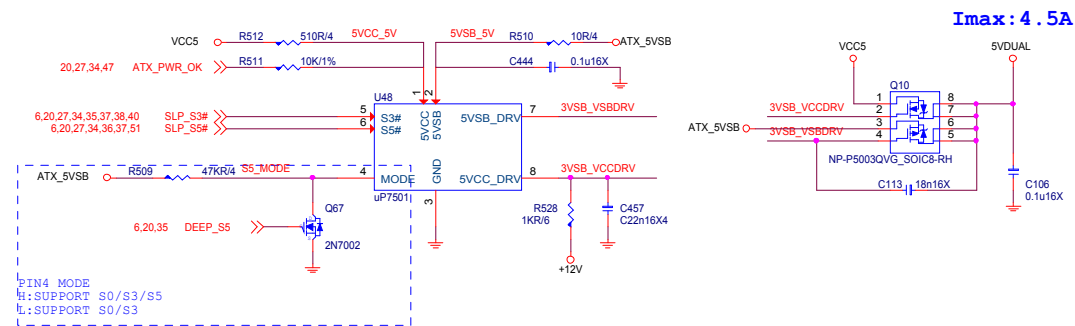
 MSI <small>Micro-Star International</small> <i>Link to the Future</i>			MICRO-START INTL CO.,LTD.		
Title DP to VGA RT6516					
Size Custom	Document Number MS-7B87				Rev 11
Date: Monday, June 25, 2018		Sheet 33		of 56	

5VDIMM FOR DDR

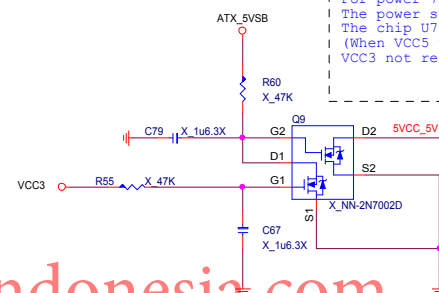


VCC_DDR需做能記錄前一次超壓設定於S5之下的控制
使用SIO GPIO54控制5VDIMM於S5下有電,SIO留0 ohm

5VDUAL For 3VSB、CPU 1.8V、VDDP

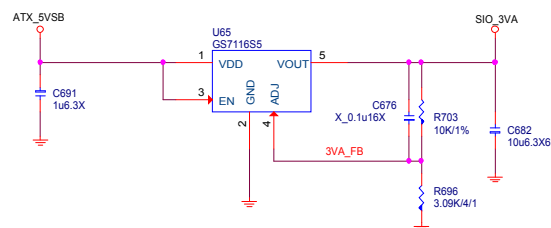


```
| For power 700W solution (only for uP7501+uP7506 for 3VSB solution)|
| The power supply VCC3 delay 12ms after VCC5 assert.             |
| The chip U7501 5VDRV1 work when the VCC5 ready                  |
| (When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but    |
| VCC3 not ready and let the 3VSB sequence fail.                  |
```

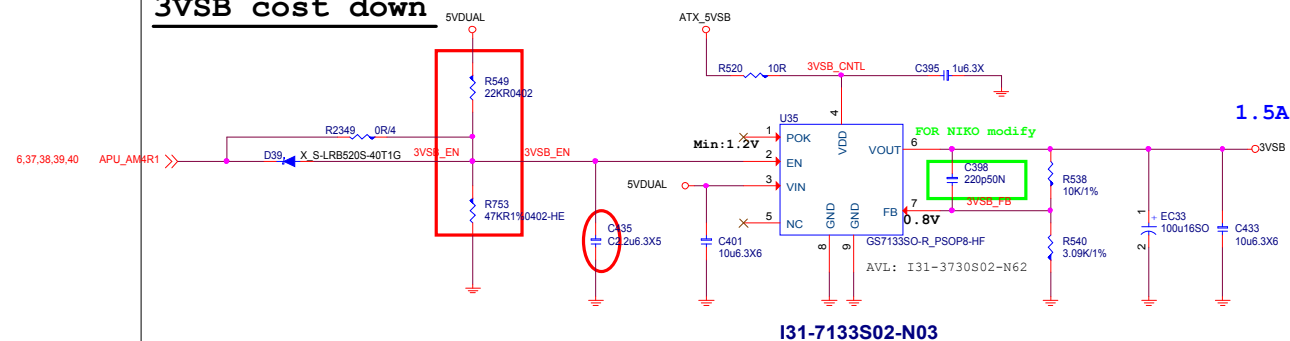


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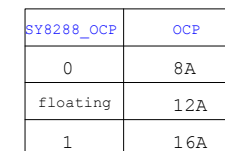
SIO_3VA



3VSB cost down

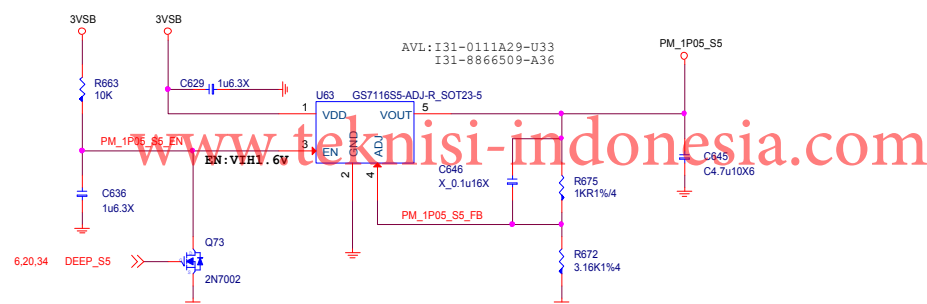


1.05V
S0:5.5A
S5:0.05A

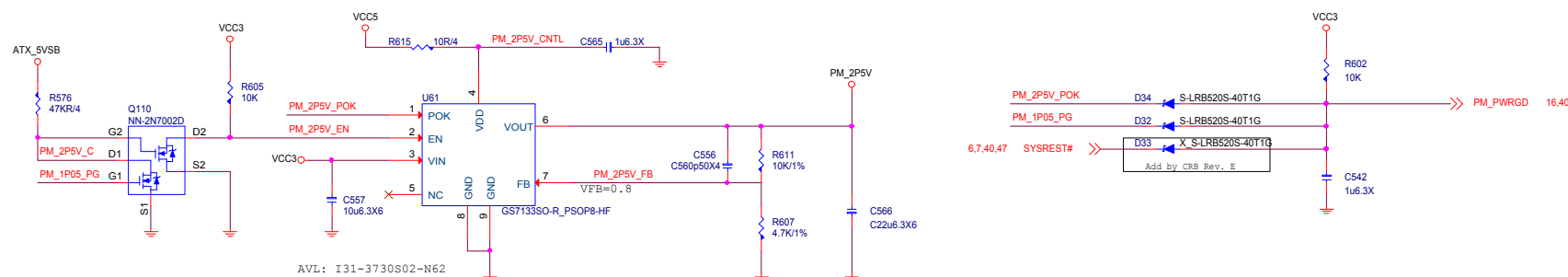


$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.6 * (1 + (1K/1.33K)) \\ &= 1.051V \end{aligned}$$

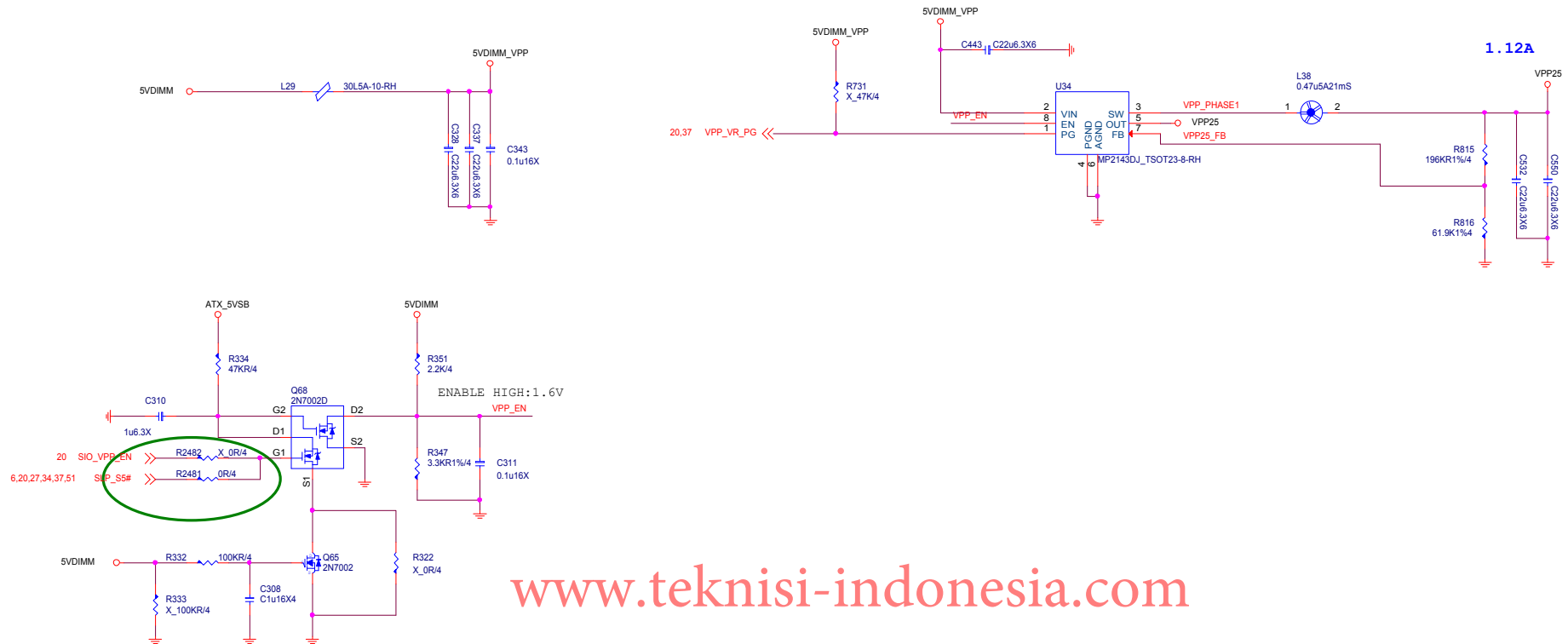
0.05A



2.5V; 900mA



2DIMM :1.12A FOR DDR VPP2.5V



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DDR4_1.2V 15.5A+4.75A+0.6A=20.85A
15.5A FOR CPU
4.75A FOR 2DIMM
0.6A FOR DDR VTT

$$I_{rms} = I_{out} * \sqrt{D/N - (D)^2}$$

$$V_{CCDDR} = V_{out}/V_{in} = 1.2/5 = 0.24$$

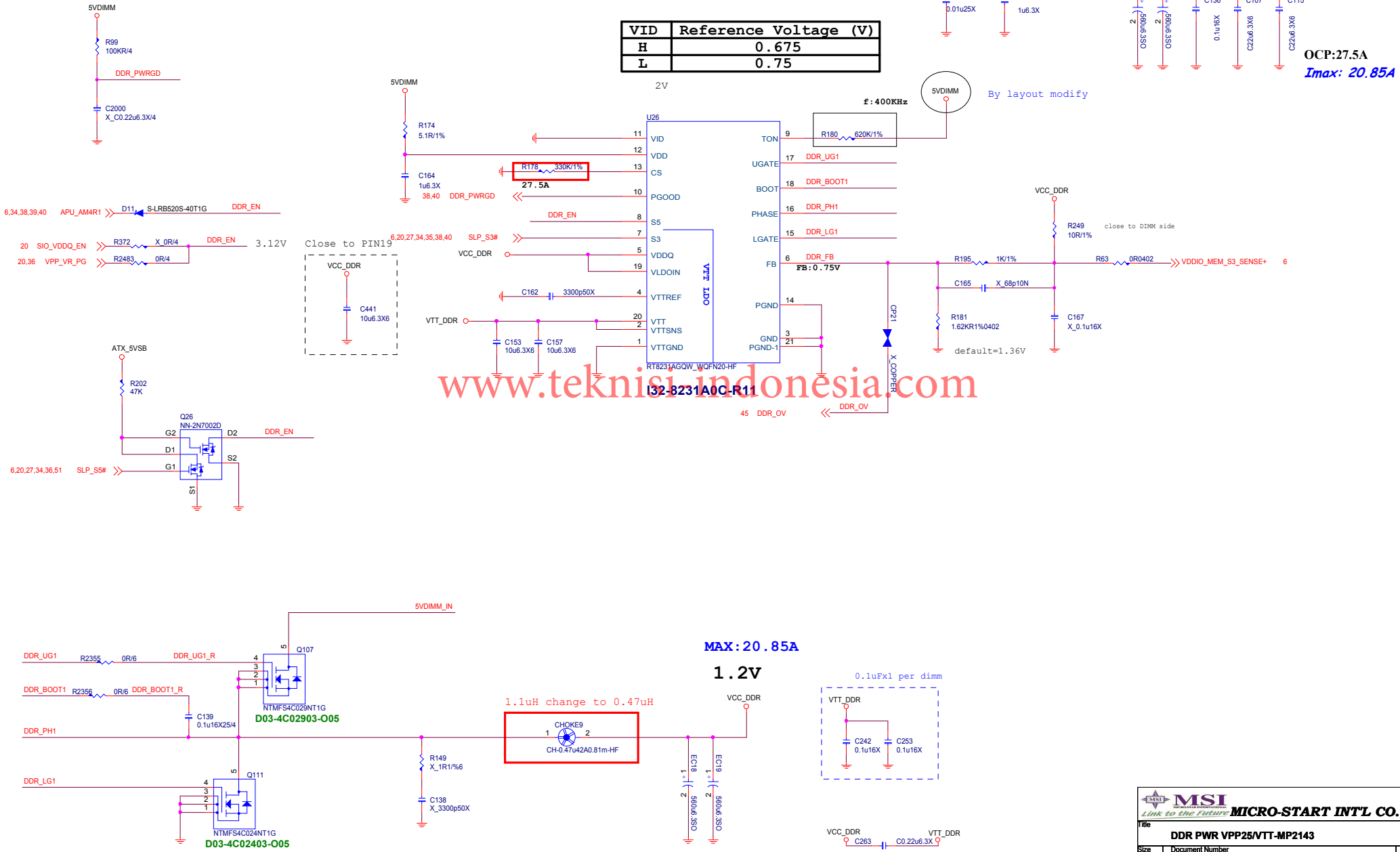
$$N = \text{Phase number} = 1$$

$$= 20.85A * \sqrt{0.24 - 0.0576}$$

$$= 5.21A$$

VID	Reference Voltage (V)
H	0.675
L	0.75

OCP:27.5A
Imax: 20.85A

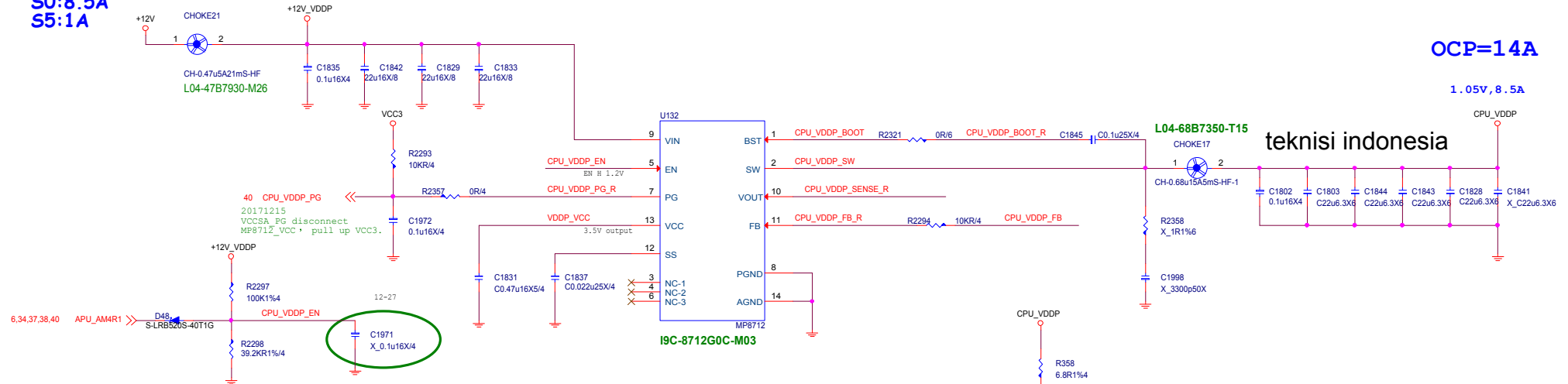


CPU_VDDP_S0

1.05V/0.9V@S0:8.5A

S0:8.5A
S5:1A

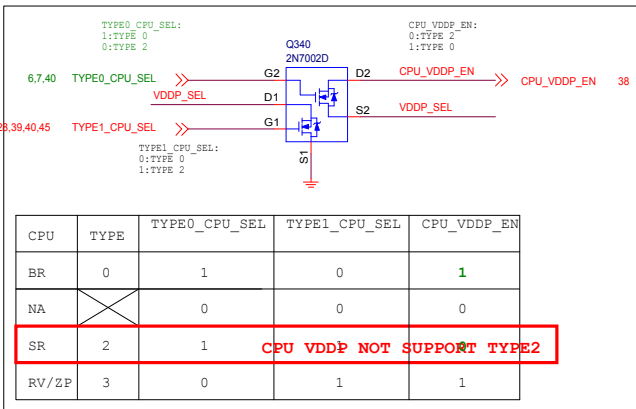
OCP=14A



OCP=14A

1.05V, 8.5A

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AM4_CPU_SEL
0:Type 0/1 =>1.053V
1:Type 2/3 =>0.9V
5,6,28,39,40,45 TYPE1_CPU_SEL

PM_GPIO_R9
Page 17 pull high
1:Type 0/1 1.05V
0:Type 2/3 0.9V

Type 0/1:
 $V_{out} = V_{ref} * (1 + (R1/(R2//R3)))$
 $= 0.6 * (1 + (1K/(2K//3.83K)))$
 $= 1.056V$

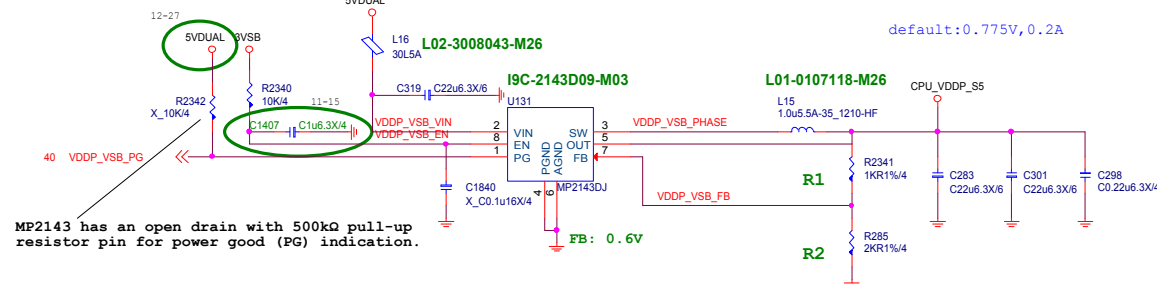
Type 2/3:
 $V_{out} = V_{ref} * (1 + (R1/R2))$
 $= 0.6 * (1 + (1K/2K))$
 $= 0.9V$

CPU_VDDP_S5

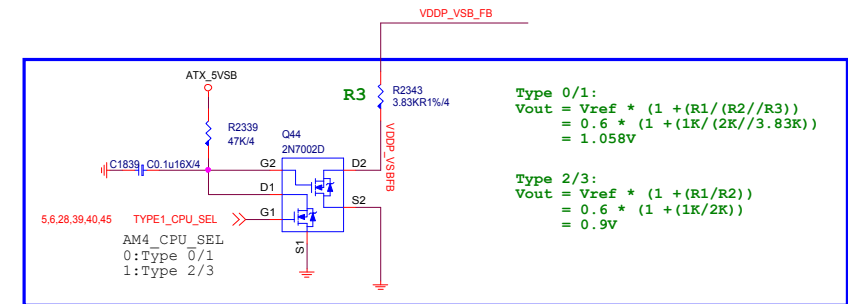
1.05V/0.9V
S5:1A

Input Current=0.04A

default:0.775V, 0.2A

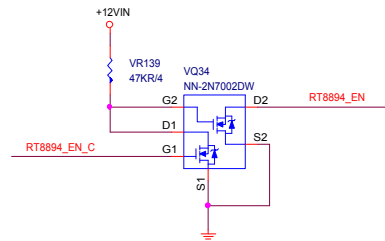


MP2143 has an open drain with 500kΩ pull-up resistor pin for power good (PG) indication.

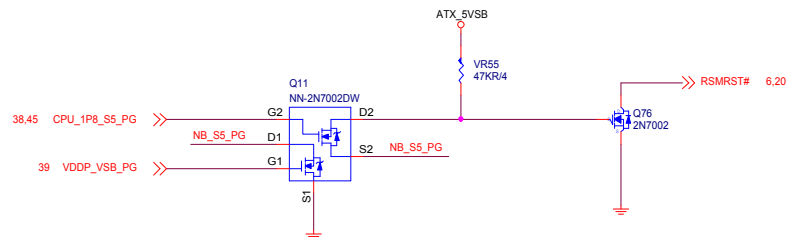


Type 0/1:
 $V_{out} = V_{ref} * (1 + (R1/(R2//R3)))$
 $= 0.6 * (1 + (1K/(2K//3.83K)))$
 $= 1.058V$

Type 2/3:
 $V_{out} = V_{ref} * (1 + (R1/R2))$
 $= 0.6 * (1 + (1K/2K))$
 $= 0.9V$

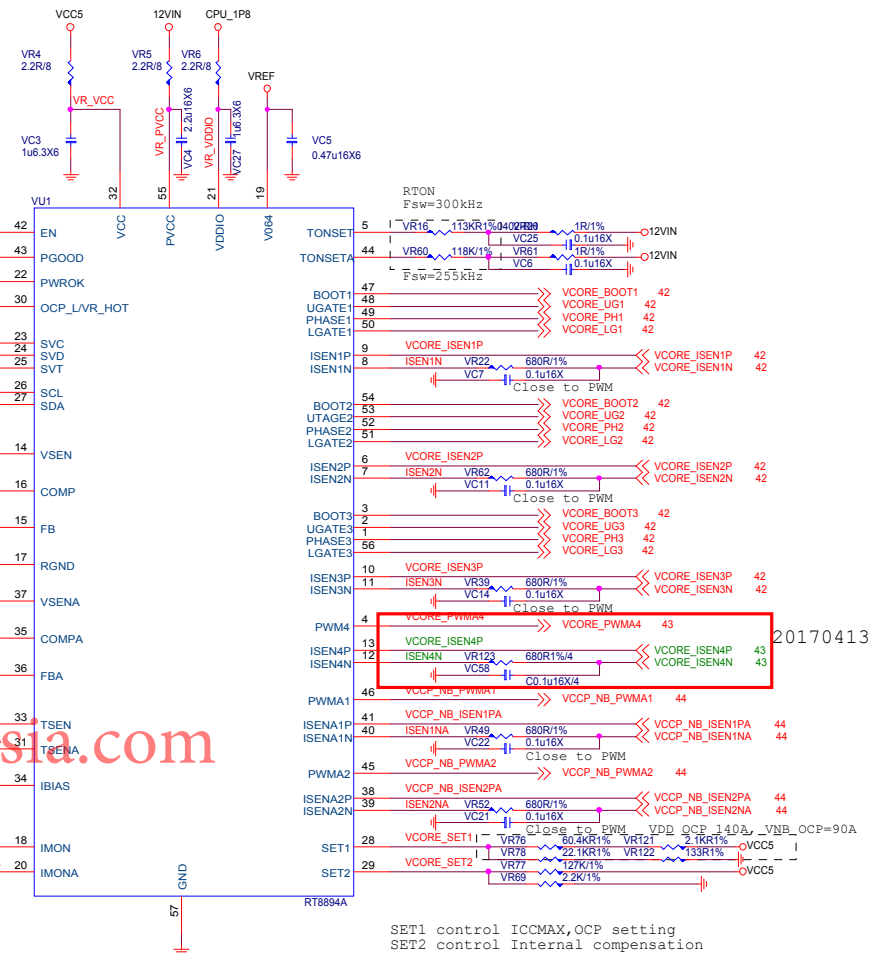
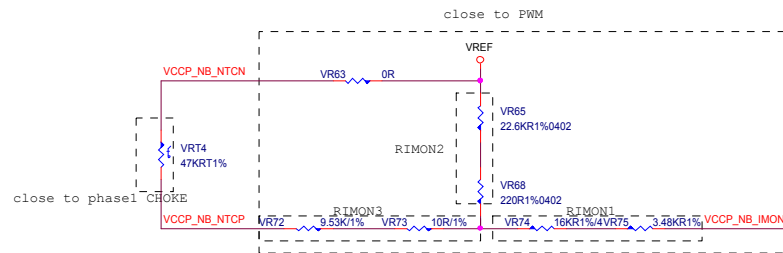
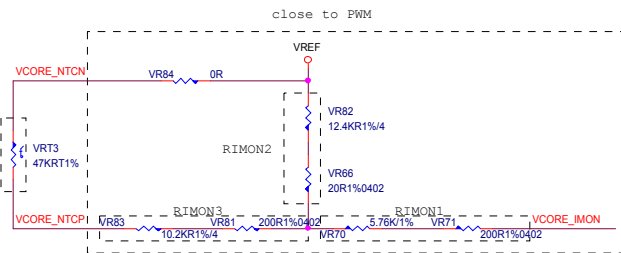
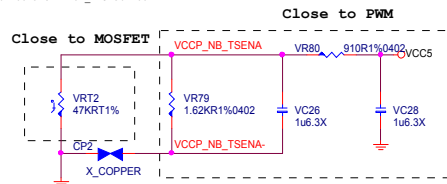
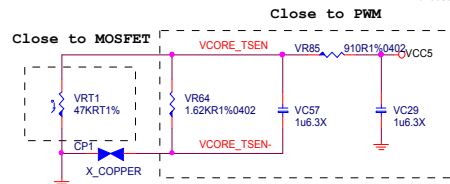
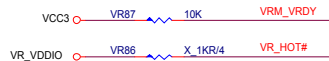
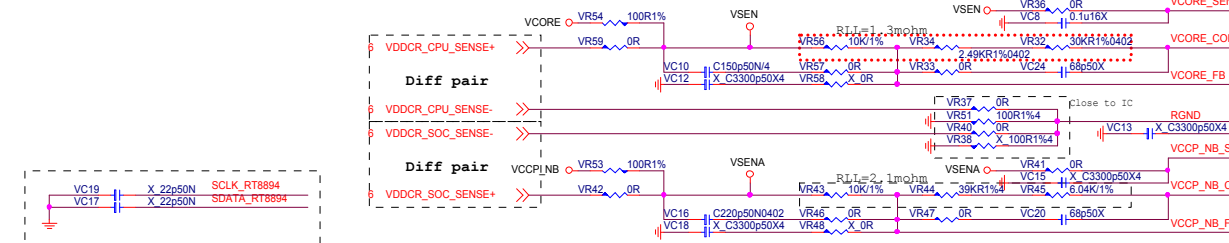
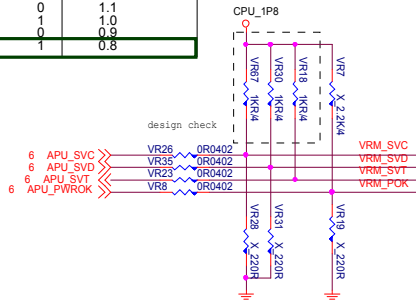
[illegible]

S5 PG

[illegible]


When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100K
If you're buffer use 3.3V_S5 and you don't need PD.

		BOOT VOLTAGE
SVC	SVD	Pre PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

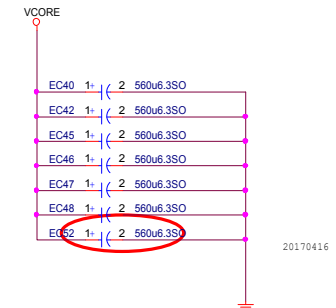
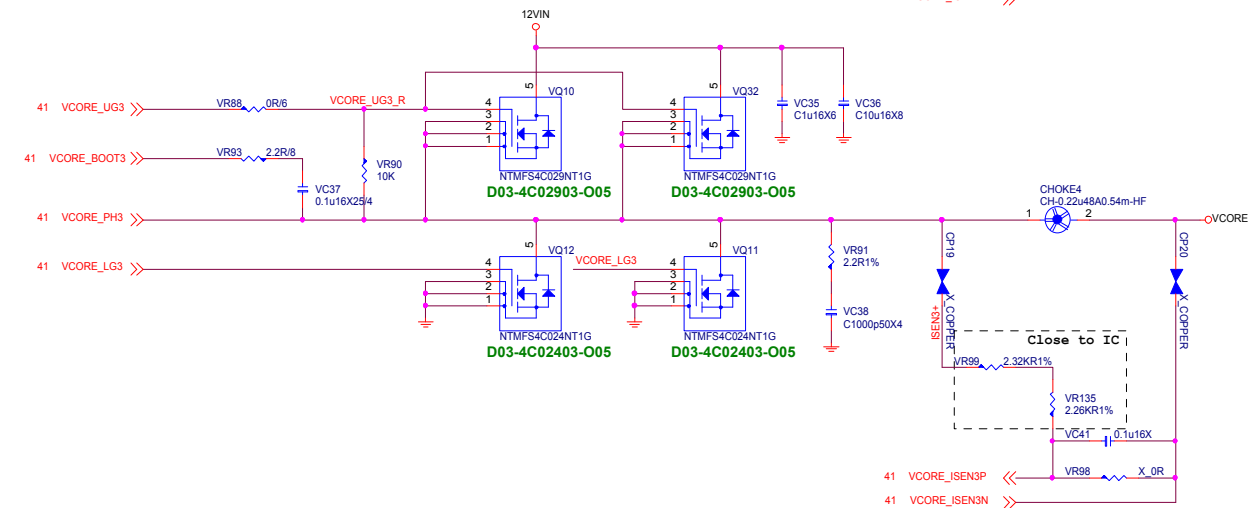
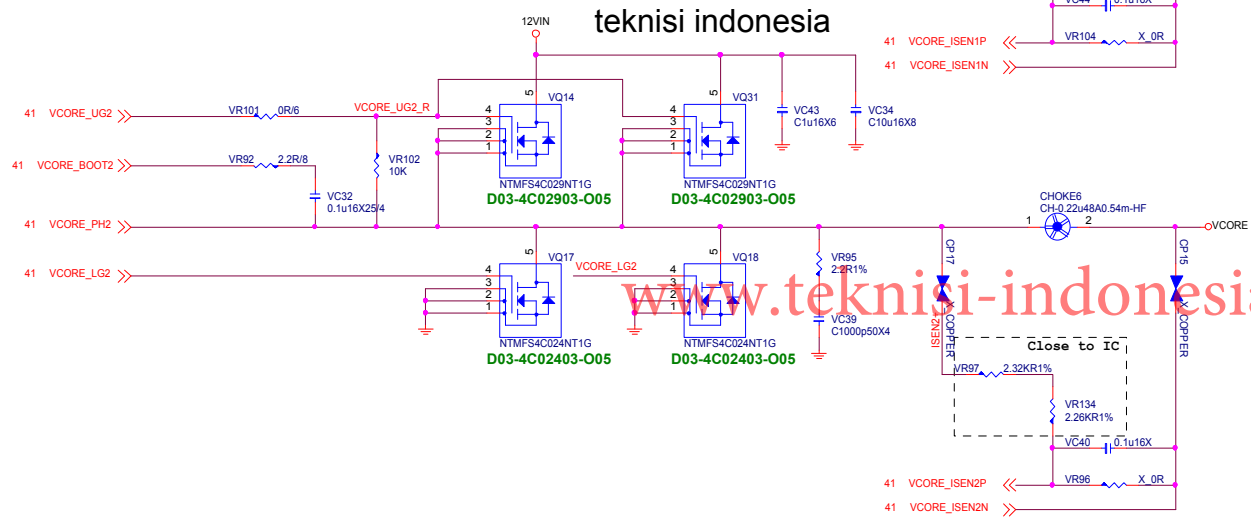
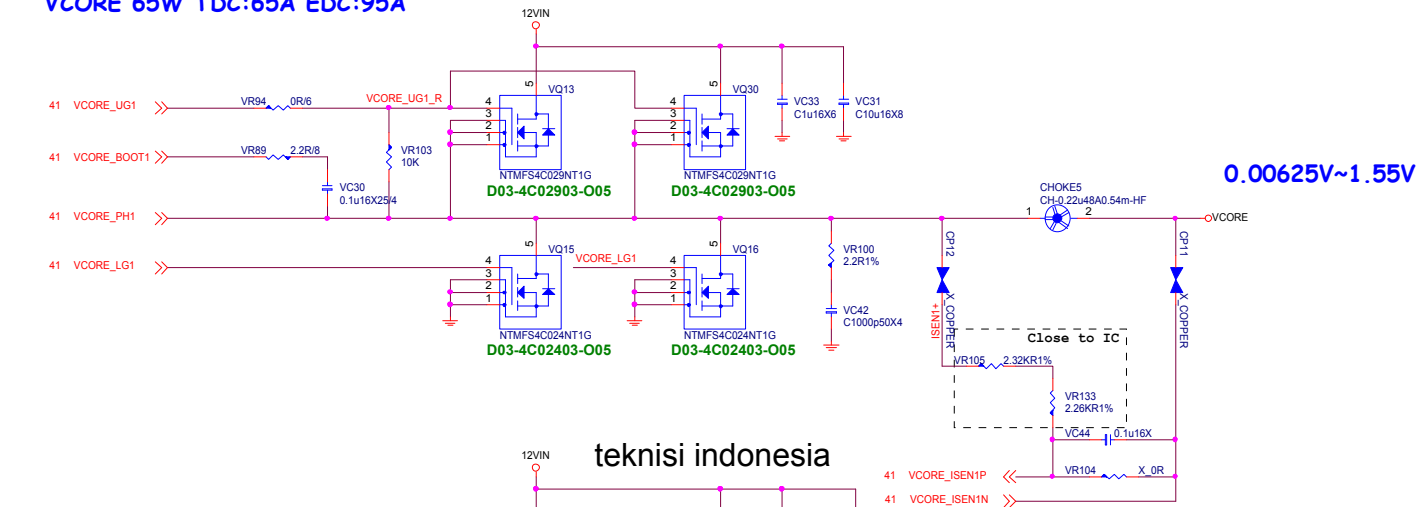


```
VCORE IccMAX: 125A =>OCP=>140A
VCC NB IccMAX: 75A =>OCP=> 90A
```

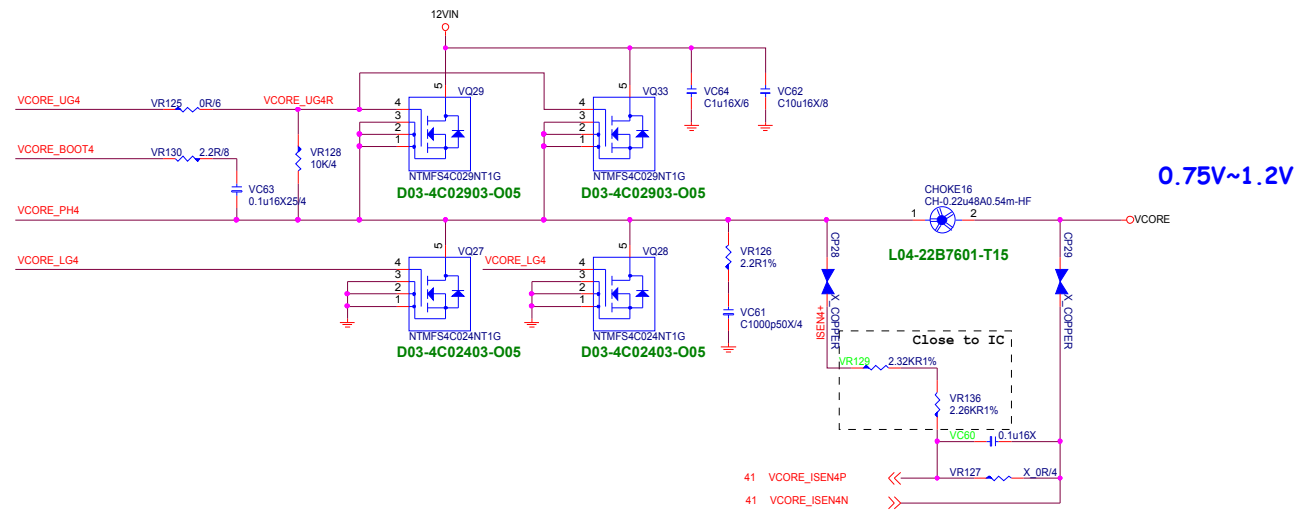
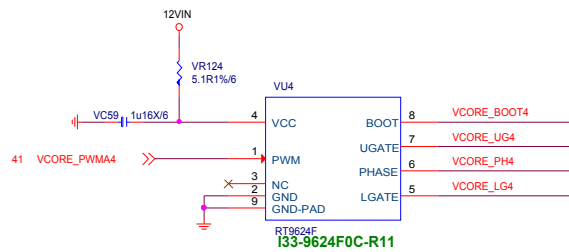
SMB Address: 0X40

 MSI <i>Link to the Future</i>				MICRO-START INTL CO.,LTD.			
File							
CPU Power RT8894 4+2 Phase							
Size		Document Number				Rev	
Custom		MS-7B87				11	
Date:		Monday, June 25, 2018		Sheet		41 of 56	

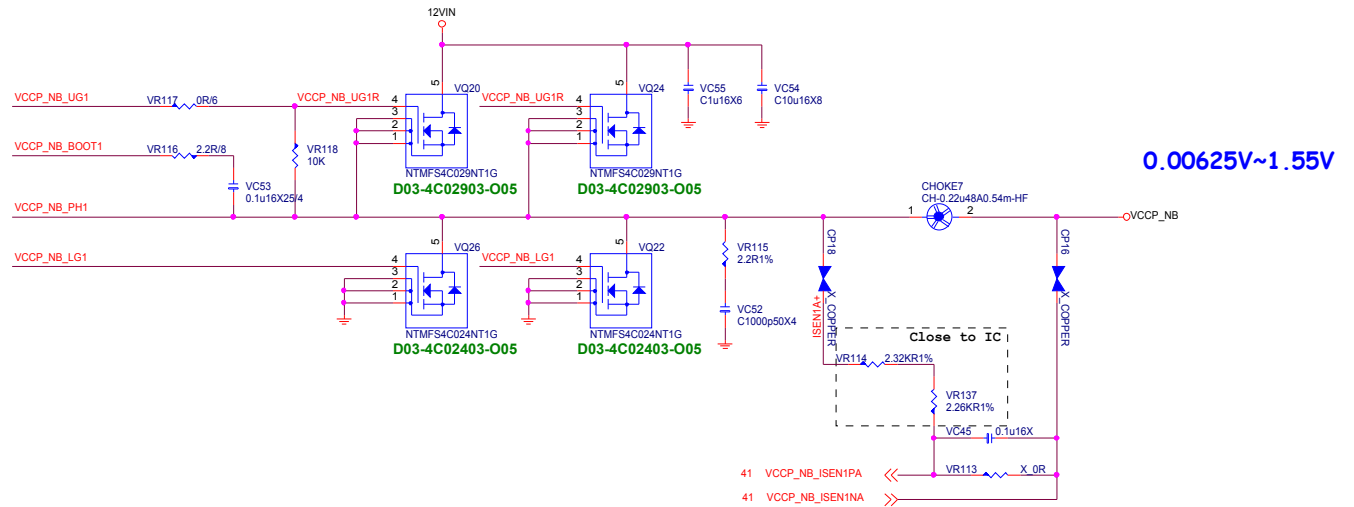
VCORE 95W TDC:80A EDC:125A
VCORE 65W TDC:65A EDC:95A



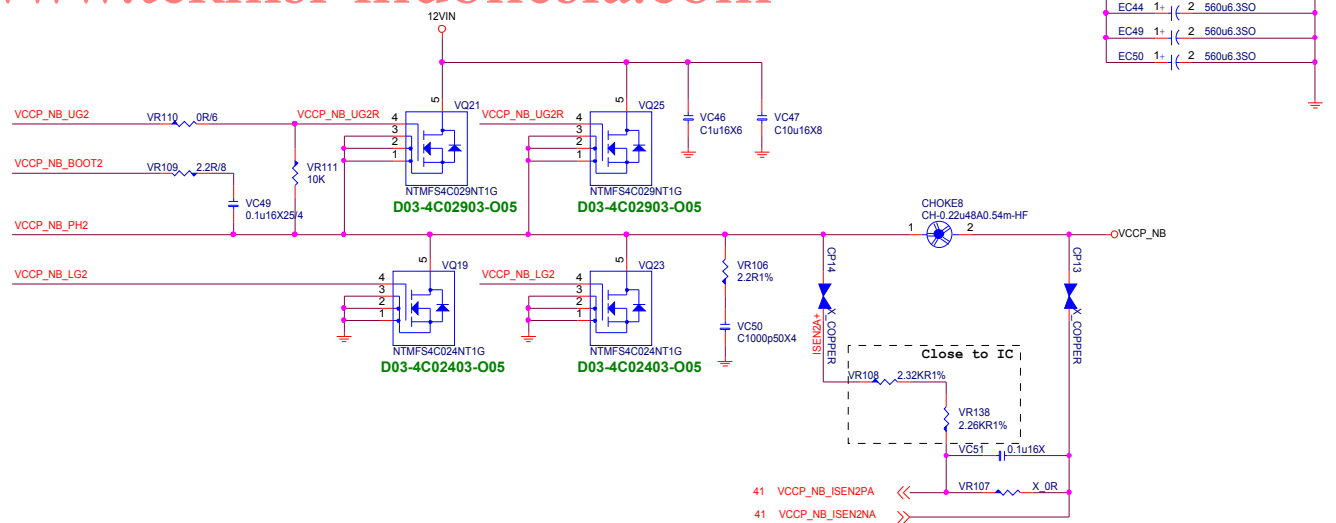
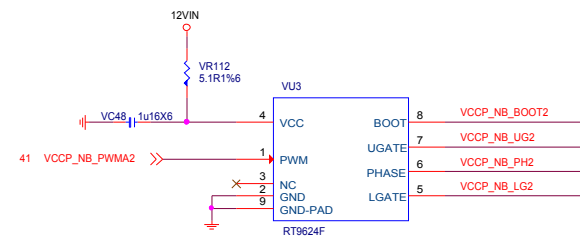
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FOR
VCCP_SOC_S5
0.9A

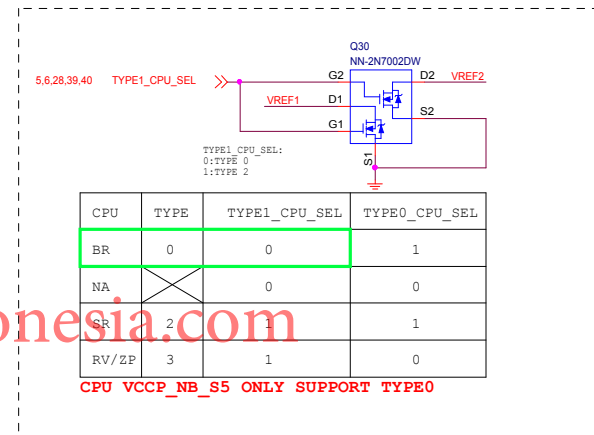
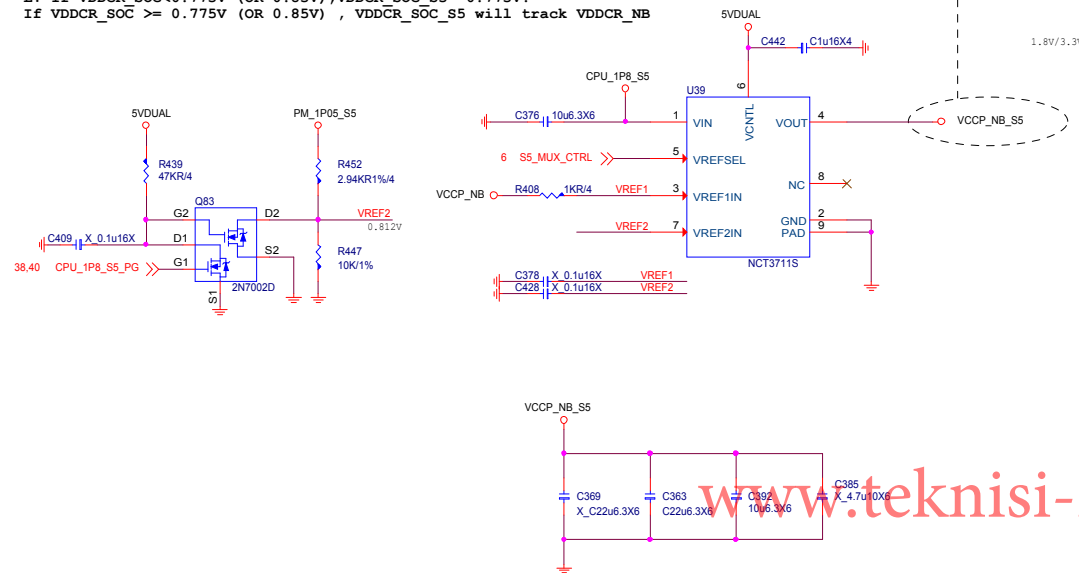
(VDDCR_SOC_S5 is only used for AMD TYPE0)

TYPE0 Only

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

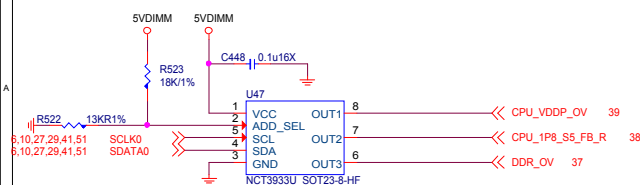
H: +VDDCR_FCH ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V), VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors) Bristol Ridge TYPE0

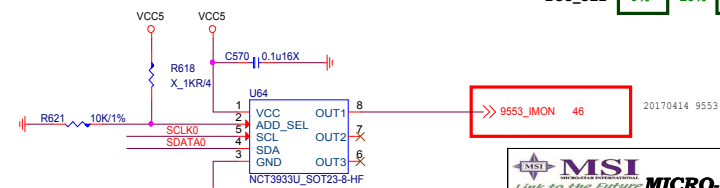


Over Voltage Control IC

0x26: RH=18K, RL=13K

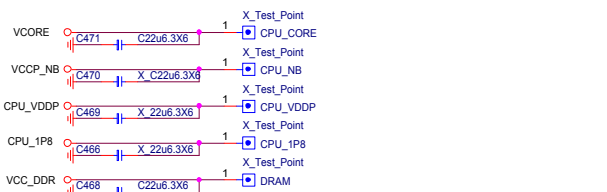
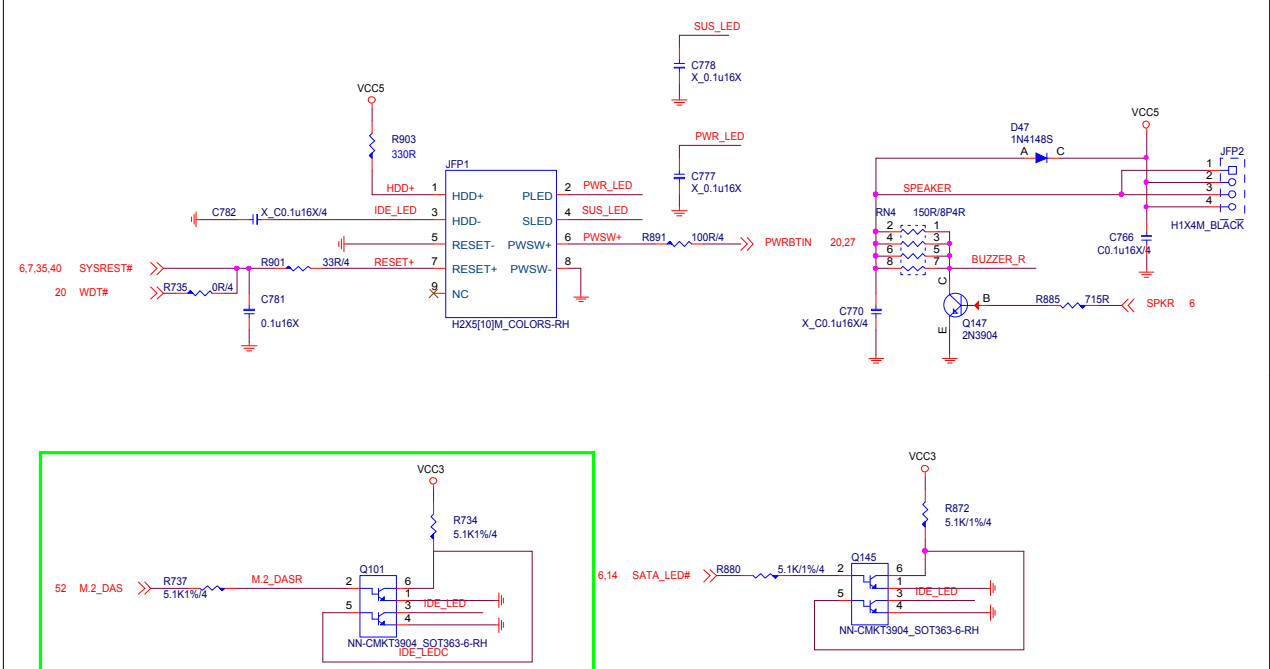
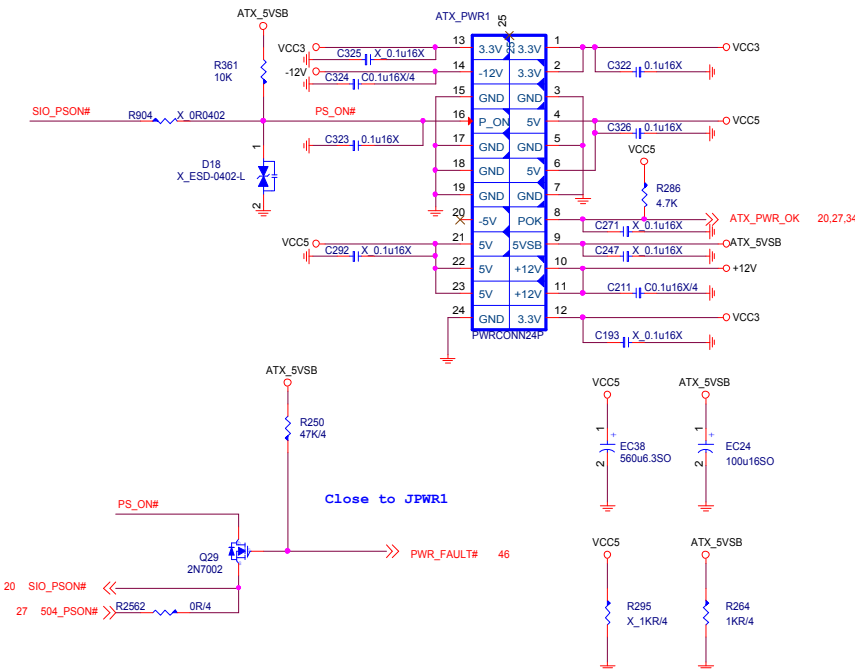


0x2A: RH=OPEN, RL=10K

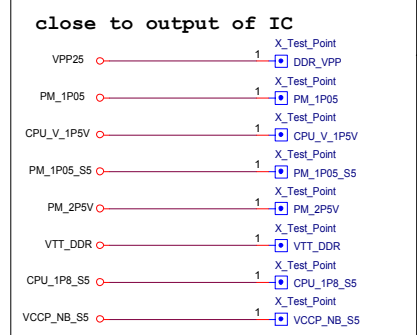
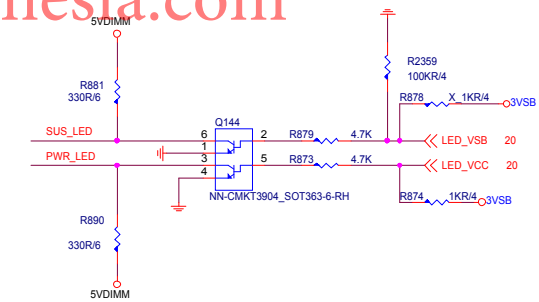
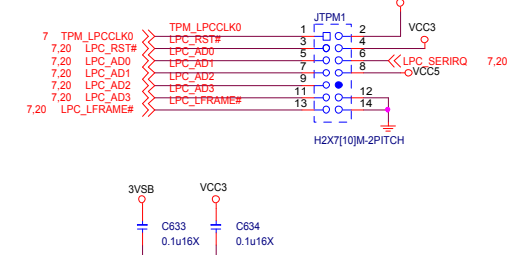


UPI VOLTAGE CONSOLE

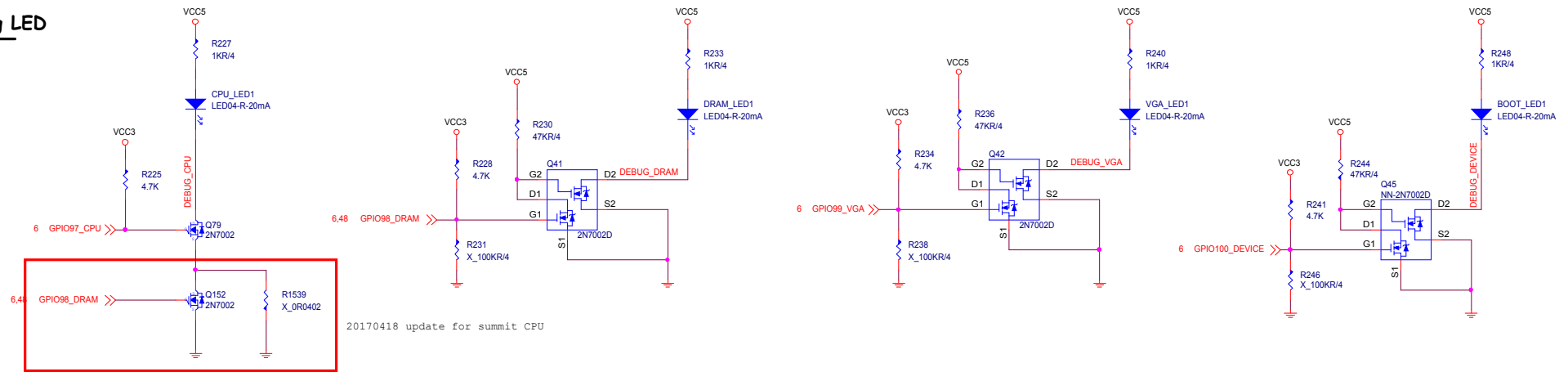
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



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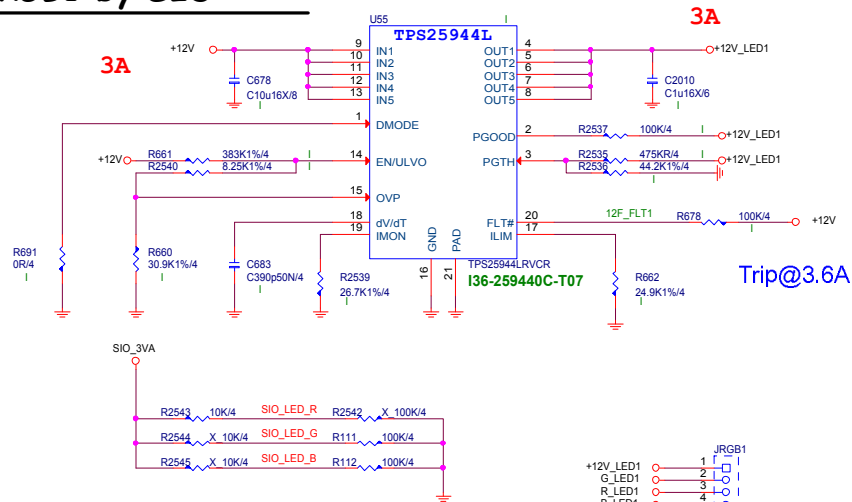
EZ Debug LED



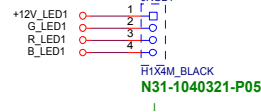
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JRGB1 by SIO

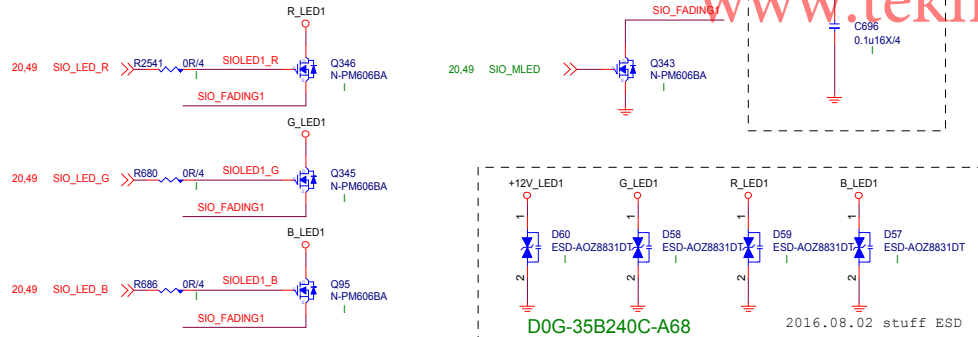
2016.07.06 Use TPS25944L



Color	SIO_LED_R	SIO_LED_G	SIO_LED_B
RED	1	0	0
GREEN	0	1	0
BLUE	0	0	1
WHITE	1	1	1

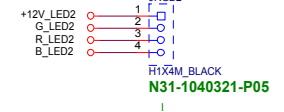
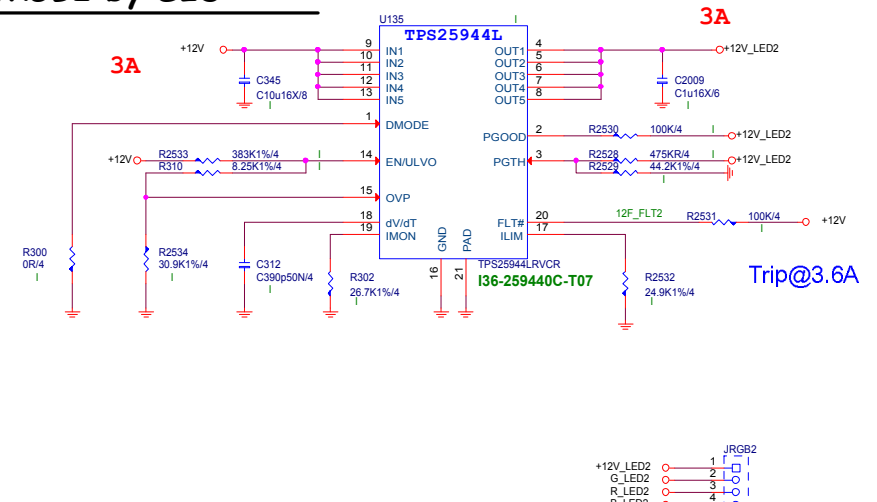


2016.08.02 Add +12V_LED 0.1uF

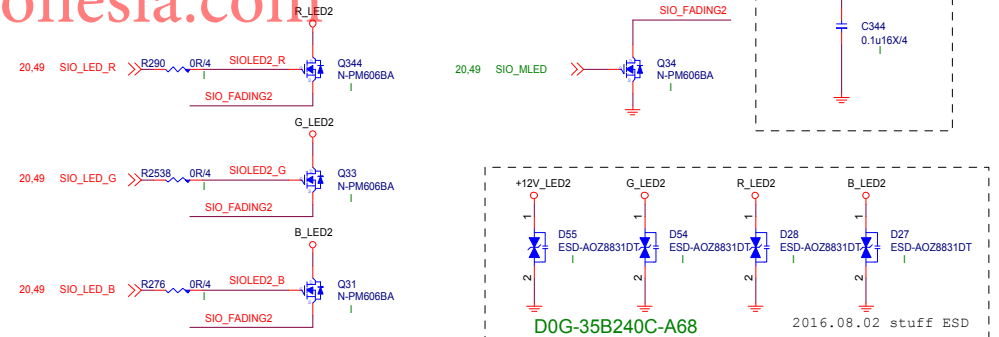


JRGB2 by SIO

2016.07.06 Use TPS25944L

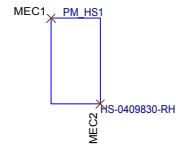


2016.08.02 Add +12V_LED 0.1uF

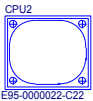


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HEAT SINK

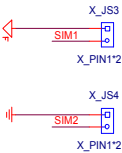


CPU Socket

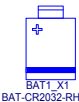


RETENTION MODULE

Simulation



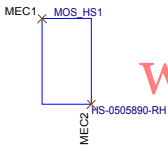
MANUAL PART



PK0-07B8411-G37, 精英-系列, 23, 寶安思斯通微 (MSIS)
PK0-07B8411-B48, 精英, 23, 寶安思斯通微 (MSIS)



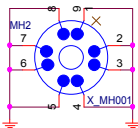
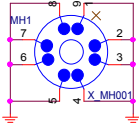
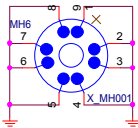
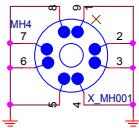
MOS HS(VCORE)



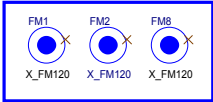
www.teknisi-indonesia.com



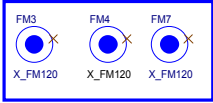
Optics Orientation Holes



5010



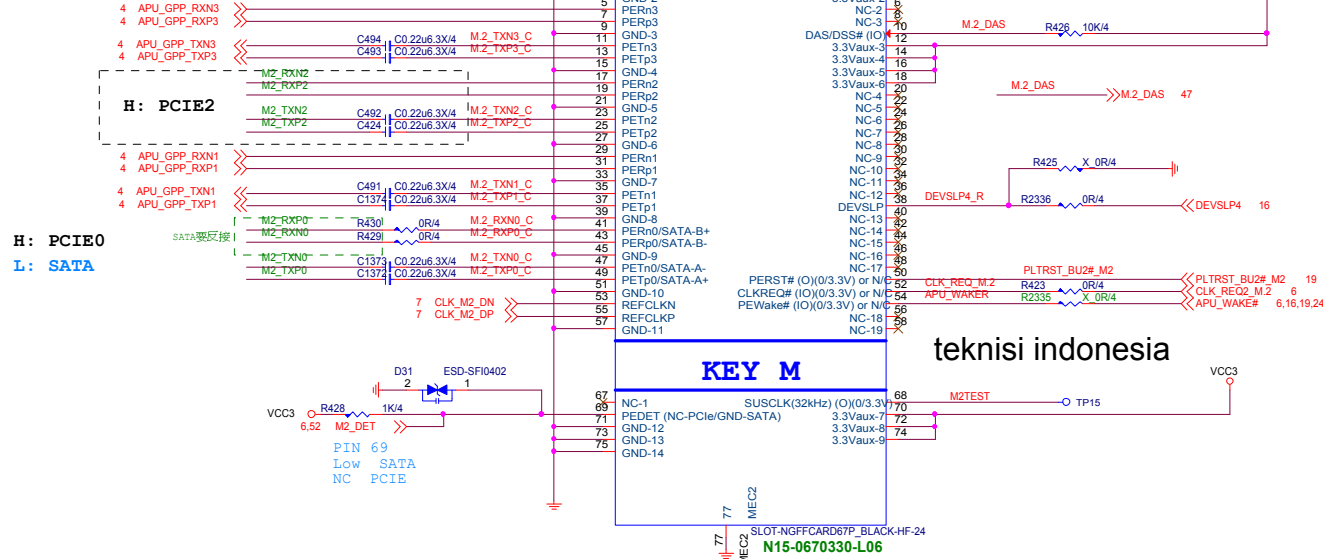
5020



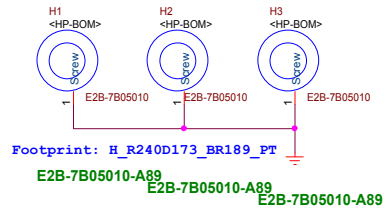
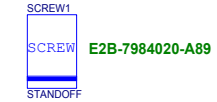
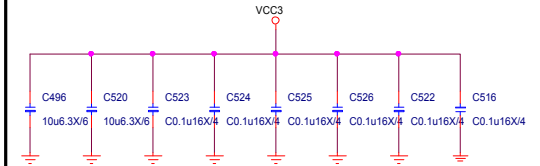
OPT	Configure	BOM	Function
		601-7B84-A01	XXXX

M.2 Connector

3.3V@2.5A



3.3V@2.5A



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M.2 Switch

